IBM®

Field Engineering
Manual of Instruction

29 Card Punch, with Left-Zero Insertion

Preface

- This manual describes only the IBM 29 Card Punch, with Left-Zero Insertion.
- For detailed descriptions of the mechanical and electrical principles of operation, see IBM 29 Card Punch, Field Engineering Manual of Instruction, Form 225-3358.
- For adjustments and maintenance procedures, see IBM 29 Card Punch, Field Engineering Maintenance Manual, Form 225-3357.
- For detailed description of machine functions, see IBM 29 Card Punch, Reference Manual, Form A24-3332.

A form has been provided at the back of this publication for readers' comments. If the form has been detached, comments may be directed to IBM Product Publications, Endicott, New York 13764.

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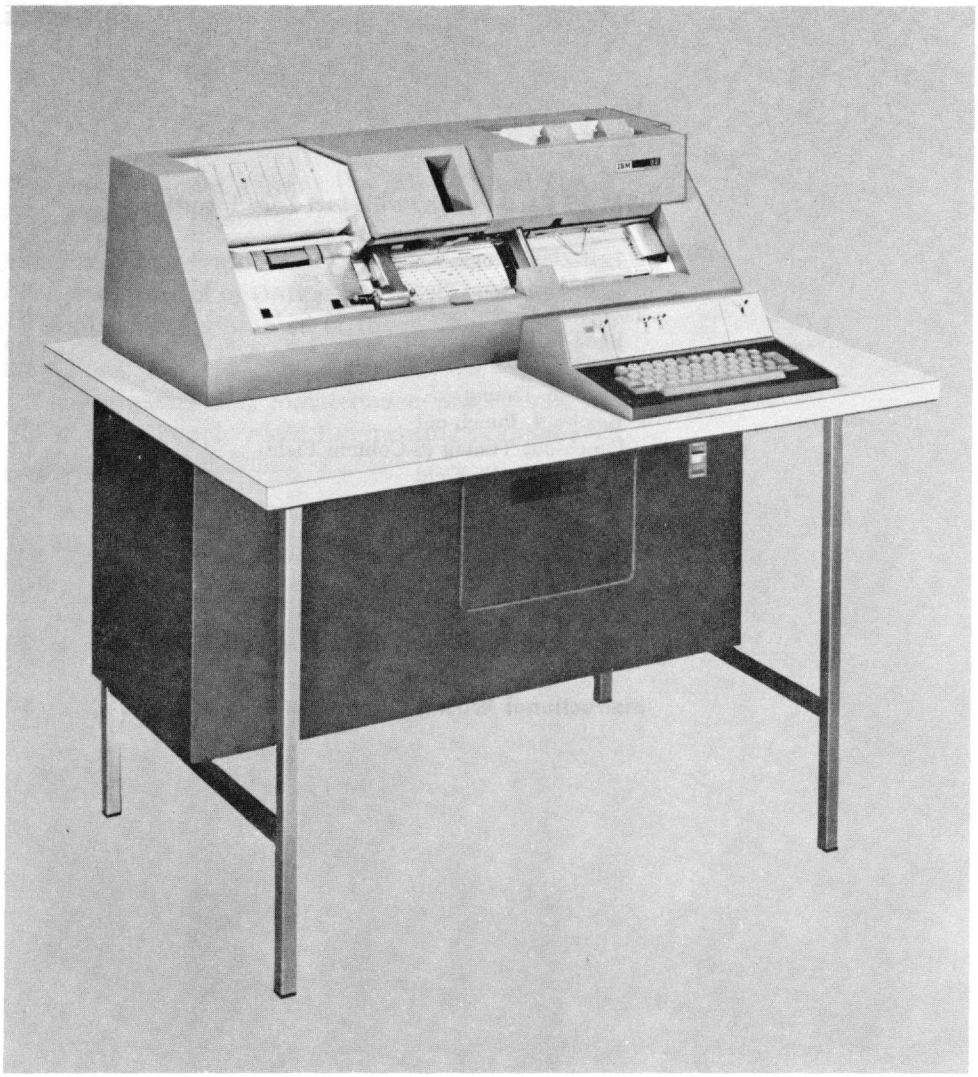


Figure 1-1. IBM 29 Card Punch, with Left-Zero Insertion

IBM 29 Card Punch, with Left-Zero Insertion

Comprehensive Introduction

- **Zeros are inserted to the left of the first significant digit.**
- **Operator keys exact number without leading zeros.**
- **Only numeric information can be entered.**
- **Keying mistakes can be corrected.**

The left-zero insertion feature permits the operator to key in only the necessary significant digits in a numeric field. The operator can then press the left-zero (or dash key for a credit field), and the machine will punch the field with the correct number of zeros in front of the significant number. Only numeric information can be entered into the left-zero field. If a key is pressed that results in punching a 12, 11, or 0 hole, plus numeric information, only the numeric information will be entered.

The left-zero feature reduces the total number of key strokes necessary to punch a field. The operator does not need to figure out the correct number of zeros to insert in front of the number. If an operator makes a mistake in keying, the field can be cleared and the correct number can be keyed in without losing information in the card.

Left-Zero Program Card

- **The size of the left-zero field is determined by the program card.**
- **A maximum of eight columns and a minimum of three columns can be programmed.**

The size of a left-zero field is determined by the program card coding (Figure 1-2). The first column of the field, high order, is punched with the correct digits to indicate field length. The remainder of the field is defined by 4's or 12's for field definition.

Left-Zero Error Reset Key

- **This key erases information stored in left-zero registers.**

When the operator presses the error reset key, the +48 volts is removed from the left-zero circuits, and all relays drop. The left-zero control relays will repick when the key is released.

	PROGRAM 1		PROGRAM 2	
Field Size	First Column	Remaining Columns	First Column	Remaining Columns
8	2	12	8	4
7	3	12	9	4
6	2-3	12	8-9	4
5	1-2	12	7-8	4
4	1-3	12	7-9	4
3	1-2-3	12	7-8-9	4

Figure 1-2. Left-Zero Program Card Coding

To make the next text and its related illustration fall on one double-page spread, this page has been left blank.

- **Key the significant number.**
- **Make corrections before the field is punched.**
- **Press the left-zero key or dash key.**

Using the program card shown in Figure 1-3, the machine stops in the high-order column of the left-zero field.

The operator can key any number of significant digits. If the operator keys more digits than the field will hold, the first digits keyed will be lost (added, or jumbled). If the wrong number is keyed or more digits than required are entered, the operator can clear the field by pressing the error reset key. Then the operator can key the correct information and punch out by pressing the left-zero or dash key.

When the operator presses the left-zero or dash keys, the machine punches out the information stored, including the necessary number of zeros.

Read-in

- **The program card coding (Figure 1-3) indicates a left-zero field.**
- **The operator presses the first digit key.**
- **A punch clutch cycle without escapement or punching is necessary.**
- **The keyboard is restored.**
- **The first digit is stored in the 8th register.**

Description

The machine is stopped at an eight-column left-zero field; the operator wishes to enter the correct digits before pressing the left-zero key. Escapement to the next column must be prevented until the left-zero key is pressed. The punch clutch is energized each cycle, but the circuit to the interposer magnets is open until the left-zero key is pressed.

To reduce the number of relays needed in each register to store the information as it is keyed, the decimal digits are converted into BCD (binary coded decimal) as shown in Figure 1-4. *Example:* Using the program card in Figure 1-3, the machine is stopped at column 10 of the program card. *The number to be keyed in this example is 46078* (Figure 1-5).

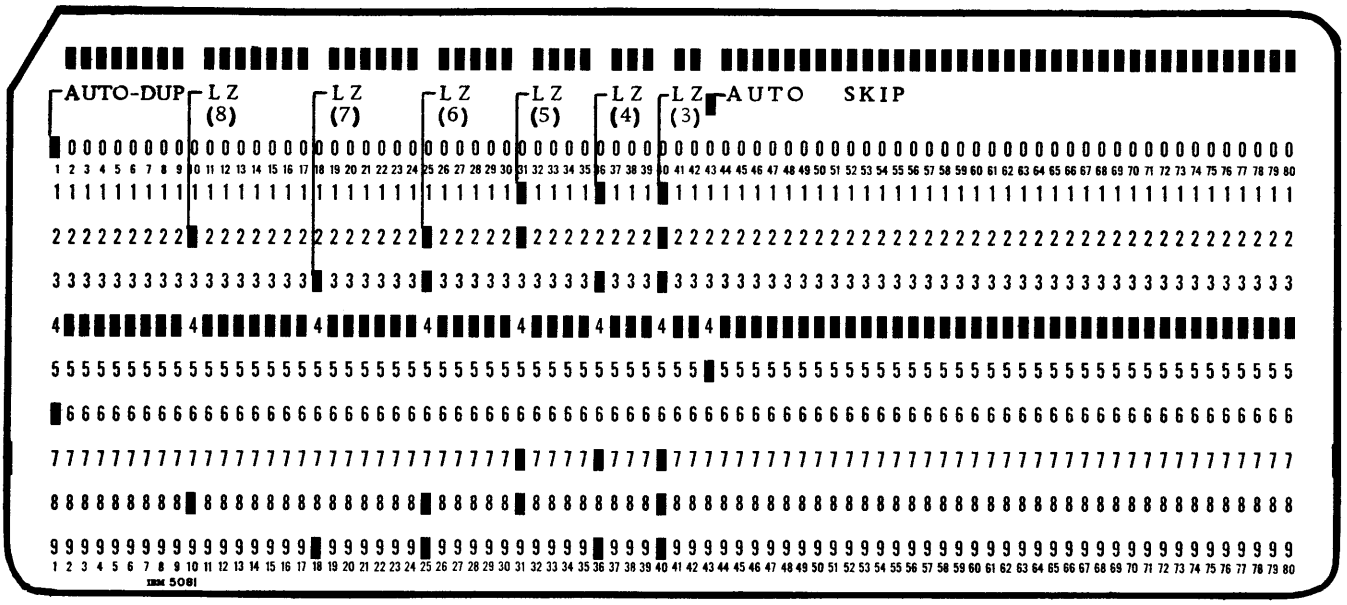


Figure 1-3. Left-Zero Program Card

Decimal	1	2	3	4	5	6	7	8	9
BCD	1	2	1-2	4	1-4	2-4	1-2-4	8	1-8

Figure 1-4. BCD Code

Cycle	Key	REGISTERS															Int. Magnet	Digit Punched	Detail Column	Program Column
		8A	8B	7A	7B	6A	6B	5A	5B	4A	4B	3A	3B	2A	2B	1A				
1 / 1	4 / LZ	4	4 / 8		7				6		4						0	-	9	10
2 / 2	6	6	6	4 / 8	4 / 8	7	7			6	6	4	4				0	0	10	11
3 / 3	0			6	6	4 / 8	4 / 8	7	7			6	6	4	4		0	0	11	12
4 / 4	7	7	7			6	6	4 / 8	4 / 8	7	7			6	6	4	4	0	12	13
5 / 5	8	8	8	7	7			6	6	4 / 8	4 / 8	7	7			6	6	4	13	14
6												8	8	7	7		0	6	14	15
7														8	8	7	7	0	15	16
8																8	8	7	16	17
9																	-	8	17	18
10																	-	-	-	-
																	Punch-Out Time Info.			

A / B — Section "A" is During Read-In Time; Section "B" is During Punch-Out Time

Note: Blank in Register Equals 0

Figure 1-5. Read-in and Punch-out (46078)

Read-in Cycle 1: Figure 1-6 is the read-in and out logic flow. Refer to Figure 1-7 for *timing* within cycles. The machine is stopped at the high-order position of the left-zero field. Starwheel 2 has been sensed, and the left-zero field relays 1, 2, and 3 (315, 324, 325) and the key-entry relay (304) are energized. These relays transfer the keyboard latch contacts from the interposer magnets to the left-zero register and allow entry of data into the registers.

The operator presses the correct key, closing the latch contact. This energizes the correct relays of the 8A register and the punch clutch. The punch clutch circuit is opened by P1 at 0°. At 20° P6 makes, energizing the keyboard restore magnets. The 8A register relays will be held by P6 or P5 until 166° when P5 breaks. The P-cam-gate relay (309) was energized at 175° by P4 of the previous cycle and is held until 79° of this cycle by P2. When P5 makes at 86°, the correct 8B relays are picked and then held until 79° of the next cycle. This transfers the information from the 8A register to the 8B register. At the beginning of the next cycle, this information will be transferred to the 7A register (Figures 1-6 and 1-7).

Field-size relays were energized at the same time the field 1, 2, and 3 relays were, but are not used when an eight-column field is keyed. Field-size relays are energized by the starwheels under control of the program card. They allow the data to enter register 8A, 7A, 6A, 5A, 4A, or 3A from the keyboard. *In our example: a 4 was stored in the 8B register* (Figure 1-6).

Read-in Cycle 2: The machine is still in the high-order column, field 1, 2, and 3 relays (315, 324, 325) are up and the key-entry relay (304) is up.

The operator presses the next key, closing the latch contact. This energizes the punch clutch and the correct 8A register relays. At 10° P3 makes, and the information being held in register 8B will be transferred to register 7A. The information in registers 8A and 7A will be held until 166° when P5 breaks. When P6 made at 20°, the keyboard was restored. At 86° P5 made, transferring the information being held in register 8A and 7A to register 8B and 7B. This information will be held by P2 until 79° of the next cycle.

In our example, the operator presses the 6 key, entering it into 8A register. The 4 in register 8B is transferred to register 7A. At 86° the 6 in 8A and the 4 in 7A are transferred to 8B and 7B.

Read-in Cycle 3: Conditions are the same as in the previous cycle. The operator presses a key. The correct relays are energized in register 8A, and a punch clutch cycle is taken. The information in the B-register is transferred to the A-registers at 10°. The information is then transferred to the B-registers at 86°. *In our example,* the operator presses the 0 key, closing the latch contact. This energizes the punch clutch through the N/O 2-point of the key-entry relay (204). Nothing is entered in register 8A, because nothing (no relays picked) in a register represents a 0 during a punch-out cycle. Information in the B-registers transfers at 10° to the next A-registers (Figures 1-6 and 1-7), and

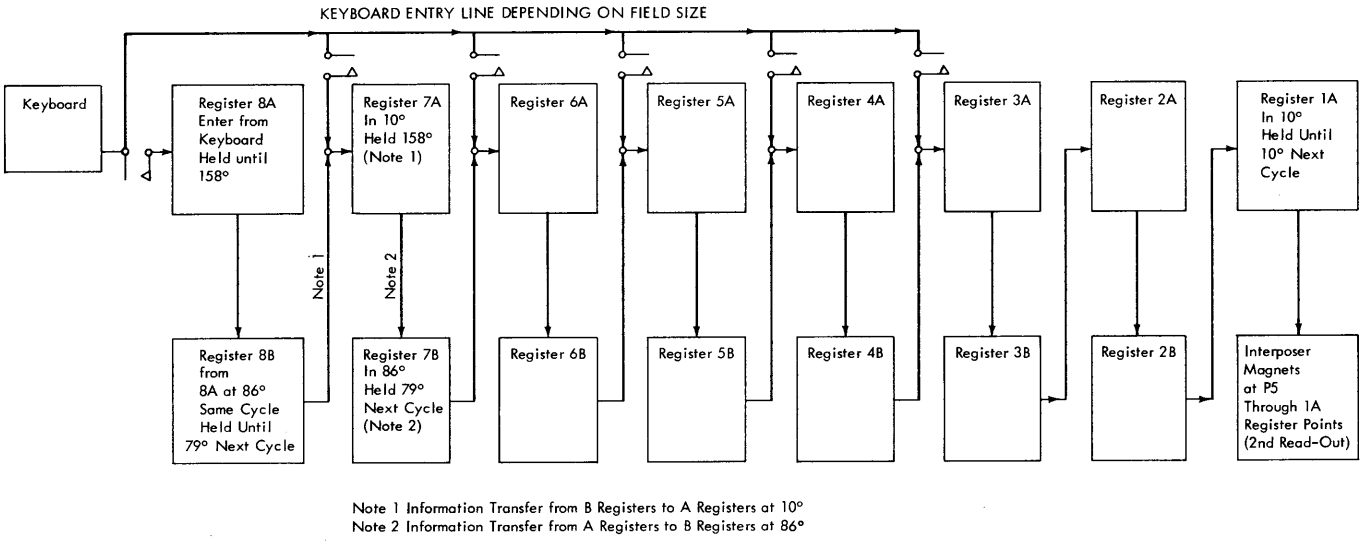


Figure 1-6. Read-in and -out Logic Flow

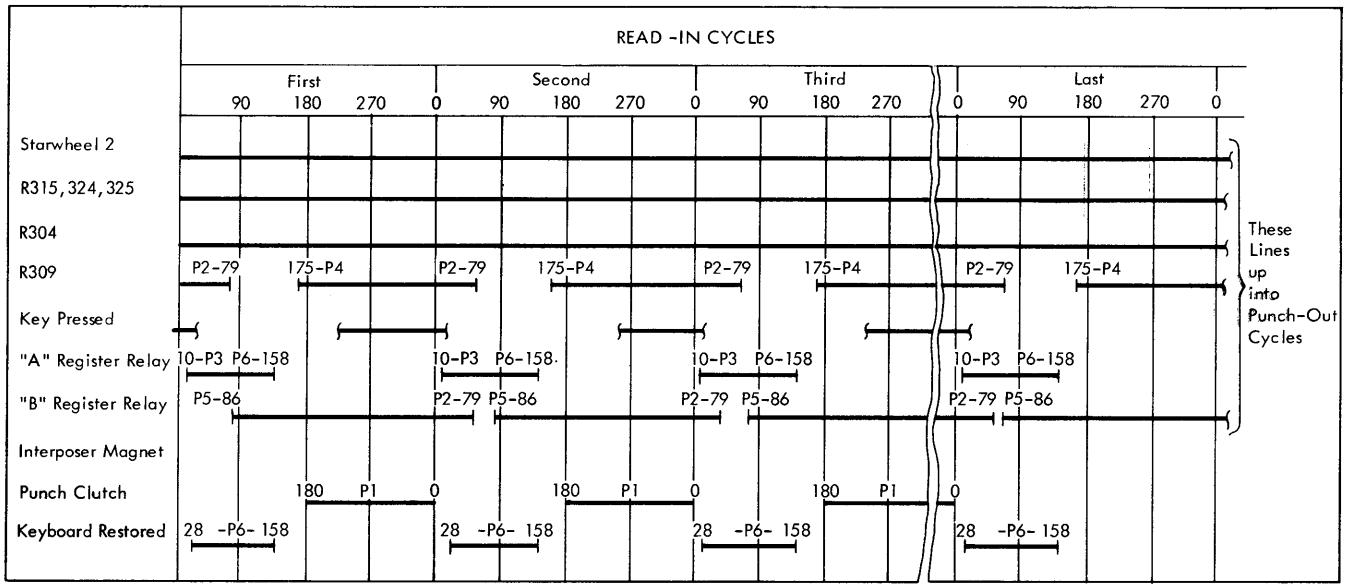


Figure 1-7. Read-in Timing

at 86° the information is transferred to the B-registers. At the end of this cycle, there is a 0 in 8B, a 6 in 7B, and a 4 in 6B.

Read-in Cycle 4: The same conditions exist as in the previous cycles. The operator presses a key, closing a latch contact. The punch clutch is energized and the correct relays in register 8A are energized. Register 8A is held until 166° by P5. The keyboard is restored by P6 at 20°. The information transfers to registers 7A, 6A, and 5A at 10°. The information transferred to the A-registers at 10° is transferred to the B-register along with the information from 8A to 8B at 86° and will be retained until 79° of the next cycle. *In our example,* the 7 key is pressed, closing the latch contact. At the end of the cycle, there is a 7 in 8B, 0 in 7B, 6 in 6B, and 4 in 5B.

Read-in Cycle 5: The same conditions are present as in previous cycles. The operator presses a key, closing a latch contact. Register 8A relays are picked as required, and the punch clutch is energized. At 10° the information in the B-registers is transferred to the next A-registers. At 86° the information in the A-registers is transferred to the B-registers. The keyboard is restored at 20°. The information in the B-registers will be retained until 79° of the next cycle. *In our example,* the operator has keyed the number 46078. The B-registers at the end of the cycle have stored an 8 in 8B, a 7 in 7B, a 0 in 6B, a 6 in 5B, and a 4 in 4B. Because registers 3B and 2B do not have any relays energized, they equal 0. All A-registers equal 0.

Circuit Objectives

1. Cycle 1 (store a 4):
   Close numeric-4 latch contact.
   Enter numeric information into register 8A and energize the punch clutch.
   Restore the keyboard.
   Transfer register 8A to 8B.
   Retain information in register 8B.
2. Cycle 2 (store a 6):
   Close numeric-6 latch contact.
   Enter numeric information into register 8A and energize the punch clutch.
   Transfer information from register 8B to 8A.
   Restore the keyboard.
   Transfer registers 8A and 7A to 8B and 7B.
   Retain information in registers 8B and 7B.
3. Cycle 3 (store a 0):
   Close numeric-4 latch contact.
   Enter numeric information into register 8A and energize the punch clutch.
   Transfer register 8B and 7B to 7A and 6A.
   Restore the keyboard.
   Transfer information from registers 8A, 7A, and 6A to 8B, 7B, and 6B.
   Retain information in registers 8B, 7B, and 6B.
4. Cycle 4 (store a 7):
   Close numeric-7 latch contact.
   Enter numeric information into register 8A and energize the punch clutch.
   Transfer registers 8B, 7B, and 6B to 7A, 6A, and 5A.
   Restore the keyboard.

Transfer information from registers 8A, 7A, 6A, and 5A to 8B, 7B, 6B, and 5B.
Retain information in registers 8B, 7B, 6B, and 5B.

5. Cycle 5 (store an 8):
Close numeric-8 latch contact.
Enter numeric information into register 8A and energize the punch clutch.
Transfer registers 8B, 7B, 6B, and 5B to 7A, 6A, 5A, and 4A.
Restore the keyboard.
Transfer information from registers 8A, 7A, 6B, 5B, and 4B.
Retain information in registers 8B, 7B, 6B, 5B, and 4B.

Read-out, Punch-out

- **Read out the stored information.**
- **Set up the interposer magnets.**
- **Energize the escape and punch clutch magnets.**
- **Punch the information into the card.**

Description

The punch-out of a left-zero field is like an auto-duplication operation. It is necessary to take a punch cycle without an escapement to start the punch-out. During the time that P5 is made, the information in the first register is read into the interposers. Information in the interposers causes the first escapement and the next punch cycle.

It is necessary to prevent the transfer of information stored in the register for the first cycle (dummy cycle) to allow the first register to be read and cleared. As each column is punched, the information is transferred from register to register. This is done so the information to be punched is in register 1A at P5 time of each punch cycle. The information is stored in BCD and must be converted to decimal form before reaching the interposer magnets. This is accomplished by using register 1A relays to form a decode tree.

Read-out, Punch-out Cycle 1: Refer to Figure 1-8 for timing within cycles. The operator presses the left-zero key, closing the left-zero latch contact. This energizes the read-out relay (326) and the punch clutch.

The left-zero field 1, 2, and 3 relays (315, 324, 305) and key-entry relay (304) are being held by starwheel 2. The P-cam-gate relay (309) is up, being picked at 175° of the last cycle by P4. We would normally transfer information from the B registers to the A registers at 10° when P3 makes, but for this cycle we prevent the P3 pulse from going to the registers. This is done with the N/C 3-point of the read-out relay (326).

Because we do not transfer the information, we must hold the information in the register for this first cycle. This is accomplished by using the N/O 5-point of the read-out relay (326) and starwheel 2. By the time that an escapement has occurred and starwheel 2 opens, P2 is made, providing a hold to the B registers. When the 2-starwheel opens, the key-entry relay (304) and the field 1, 2, 3 relays (315, 324, 325) are de-energized.

The 1A register is held during the first cycle by the N/C 4-point of the punch-out relay (317) until 86° when relay 317 is picked. Relay 317 is picked by P5 through the N/O 2-point of the read-out relay (326). Before relay 317 is picked, P6 makes, providing a hold until 150° for register 1A. If the relays of register 1A were dropped at 150°, the interposer magnets circuit would be opened by relay points.

P7 provides a continuing hold to register 1A relays until 10° of the next cycle. At P5 time (86° to 166°) the interposer magnets are energized through the N/O 6-point of the read-out relay (326) and the decode tree of register 1A relay points. It is this circuit that

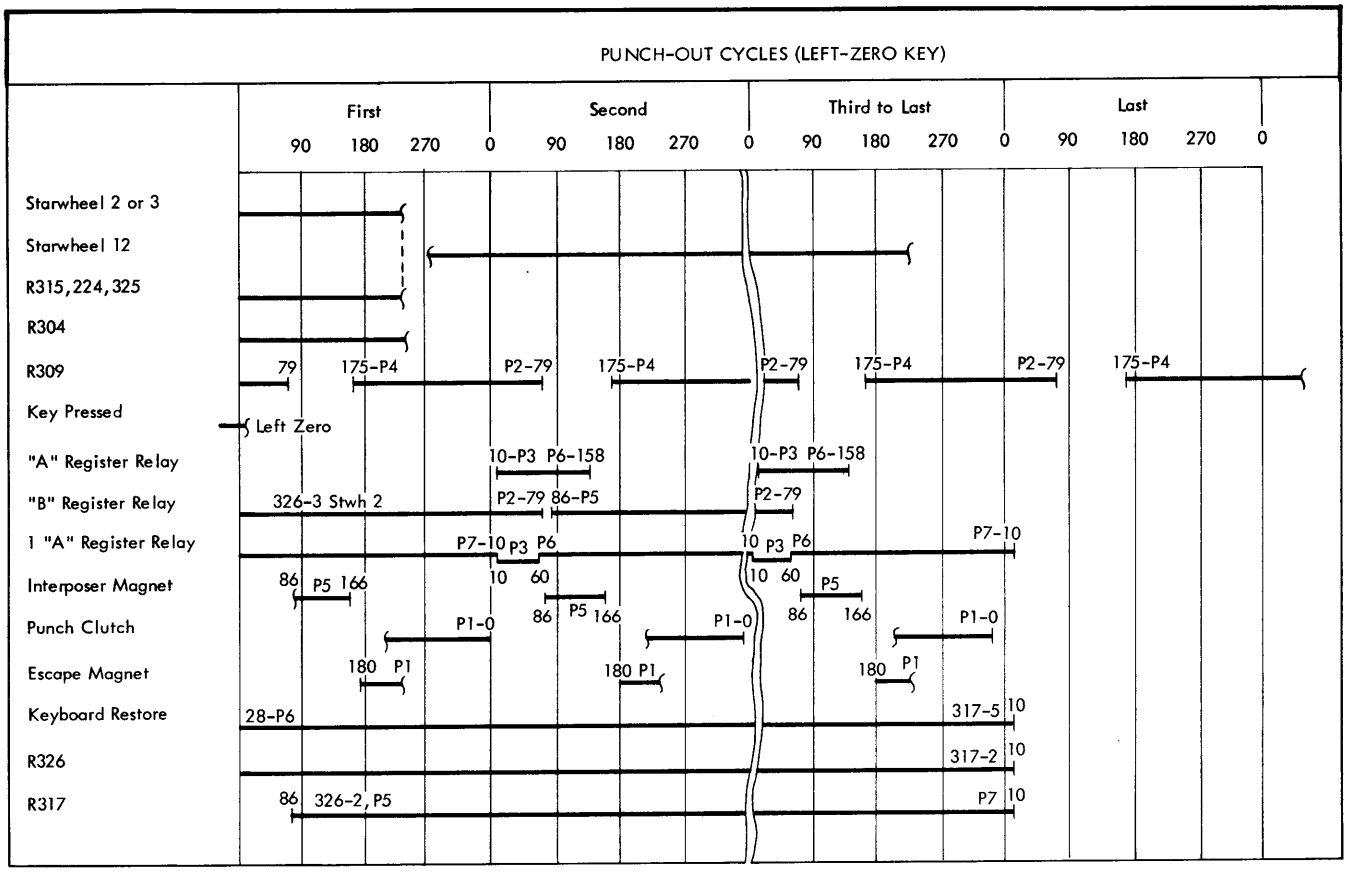


Figure 1-8. Punch-out Timing (8-Column Field)

energizes the zero interposer when the condition of no relays picked exists.

The keyboard was restored at 20° by P6 and is held restored by the N/O 5-point of the punch-out relay (317) to +48 volts, for the rest of the left-zero field. The escape magnet is energized by the interposer bail contacts, and P1 (180°). The escape armature contact makes, energizing the escape interlock relays. This allows the punch clutch to be energized for the next cycle. *In our example*, during this cycle we energized the zero interposer magnet, and escaped to column 10.

Read-out, Punch-out Cycle 2: During this cycle we punch the information that was transferred from register 1A to the interposer magnet during the last cycle. We transfer the information from register to register and energize the interposer magnet for the digit to be punched during the next cycle. The punch clutch will not latch up for the rest of the left-zero field.

At 10° the information in B-registers will be transferred to the next A-register (Figure 1-8) All A-registers are held until 166° by P6 and P5; the 1A register is held until 10° of the next cycle by P7. The transfer of information from the registers on this cycle and the rest of the punch-out cycles is allowed to occur through N/O 4 points of the P-cam-gate relay (309) and the 6-point of the punch-out relay (317) and P3.

At P5 time, the interposer magnet is energized through the decode tree. The interposer bail contacts close, energizing the escape magnet. The escape armature contact energizes the escape interlock relays. The punch clutch is energized through P1, the escape interlock points, and P2. At 86° (P5) the information in registers 8A through 2A is transferred to registers 8B through 2B and retained there until 79° of the next cycle. *In our example*, we energized the interposer 0 magnet, punched zero in column 10, and escaped to column 11 during this cycle.

Read-out, Punch-out Cycle 3: During this cycle we punch information that was set up in the last cycle, transfer new information to the interposers, escape to a new column, and initiate a punch-clutch cycle. At 10° the information is transferred from the B-registers to the A-registers. The A-registers are held until 166°, the 1A register is held until 10° of the next cycle. At 86° the information is transferred from register 8A

through 2A to register 8B through 2B. The interposer magnet is energized at 86° (P5) through the decode tree. The escape magnet is energized by the closing of the interposer bail contacts. The escape-armature contact energizes the escape-interlock relays. The punch clutch is energized through P1, the escape-interlock relays and P2. *In our example,* we punched a zero in card column 11, energized the interposer 0 magnet, escaped to column 12, and energized the punch clutch.

Read-out, Punch-out Cycles 4, 5, 6 and 7: Cycles 4, 5, 6, and 7 are identical to cycle 3 in operation. *In our example,* we punched a 0 in column 12, energized the interposer 4 magnet, and escaped to column 13 during cycle 4. During cycle 5 we punch a 4, energize the interposer 6 magnet, and escape to column 14. In cycle 6 we punch a 6 in column 14, energize the interposer 0 magnet and escape to column 15. In cycle 7 we punch a 0 in column 15, energize a 7 interposer magnet, and escape to column 16.

Read-out, Punch-out Cycle 8: During this cycle, the information set up in cycle 7 is punched, the last digit is transferred from the register 2B to register 1A. The interposer magnet is energized to allow the last digit to be punched on the next cycle. At 10° the information in register 2B is transferred into register 1A. At 86° the interposer magnet is energized through the decode tree. The interposer bail contacts make, energizing the escape magnet at 180° (P1). The escape armature contact makes, energizing the escape-interlock relays. The punch clutch is energized through P2, interlock relays, and P1. At 86° the information in registers 8A through 2A is transferred to registers 8B through 2B. All digits that were keyed in have been read out; so all registers equal zero (no relays picked). *In our example,* we punched a 7 in column 16, energized interposer 8 magnet, and escaped to column 17.

Read-out, Punch-out Cycle 9: Escapement to the last column of the field (detail card) and out of the last column of the field (program card) happened in the last part of cycle 8. This opens the starwheel 12 contact. All digits have been read out of storage, the last digit will be punched on this cycle. It is necessary to drop out the left-zero control relays during this cycle. At 10° the punch-out relay 317 is dropped; after the starwheel 12 contact opened, relay 317 was held by P7 until 10° of this cycle. The N/O 2-point of relay 317 opens, dropping read-out 1 (326). The N/O 5-point of relay 317 opens the circuit to the keyboard-restore magnets, but the interposer bail contacts hold the magnet until about 65°. The digit is punched, and the punch clutch latches at 345°. *In our example,* column 17 is punched with an 8.

Cycle	Key	REGISTERS 8A	8B	7A	7B	6A	6B	5A	5B	4A	4B	3A	3B	2A	2B	1A	Int. Magnet	Digit Punched	Detail Column	Program Column
1	4 LZ	4	4 8		7				6		4						0	-	9	10
2	6	6	6	4 8	4 8	7	7			6	6	4	4				0	0	10	11
3	0			6	6	4 8	4 8	7	7			6	6	4	4		0	0	11	12
4	7	7	7			6	6	4 8	4 8	7	7			6	6	4	4	0	12	13
5	8	8	8	7	7			6	6	4 8	4 8	7	7			6	6	4	13	14
6												8	8	7	7		0	6	14	15
7														8	8	7	7	0	15	16
8																8	8	7	16	17
9																	-	8	17	18
10																	-	-	-	-
																	Punch-Out Time Info.			

A
B

Section "A" is During Read-In Time
Section "B" is During Punch-Out Time

Note: Blank in Register Equals 0

Figure 1-9. Read-in and Punch-out Chart

Circuit Objectives

1. Cycle 1 (energize interposer 0 magnet):
   Close left-zero latch contact.
   Energize punch clutch and read-out relay (326).
   Prevent transfer of information in registers.
   Provide a hold on the information in registers.
   Provide a special hold for register 1A.
   Provide a continuous restore to the keyboard.
   Energize interposer magnet.
   Energize punch-out relay (317).
   Drop key entry (304) and field 1, 2, and 3 relays (315, 324, 325).
   Energize escape magnet.
   Energize escape-interlock relays.
   Energize punch clutch.
2. Cycle 2 (punch a 0 and energize interposer 0 magnet.
   Transfer B-registers to next A-registers.
   Hold 1A register until 10° next cycle.
   Transfer A-registers to B-registers.
   Hold B-registers' information until next cycle.
   Energize interposer magnets.
   Energize escape magnet.
   Energize escape-interlock relays.
   Energize punch clutch.
3. Cycle 3, 4, 5, 6 and 7:
   These cycles are similar to cycle 2.
4. Cycle 8 (punch a 7 in column 16 and energize interposer 8 magnet):
   Transfer B-registers to next A-registers.
   Hold register 1A information until 10° next cycle.
   Energize escape magnet.
   Energize escape interlock relays.
   Energize punch clutch.
   Break starwheel 12 or 4 contact.
5. Cycle 9 (punch an 8 in column 17):
   Drop punch-out relay (317).
   Drop read-out relay (326).
   Open circuit to keyboard-restore magnets.

Left-Zero Credit Field

To indicate a credit field, the operator keys in the information just as in a debit field. To start the read-out, punch-out operation, the operator presses the dash (—) key instead of the left-zero key. Pressing the dash key causes a credit (11 punch) in the units column to be punched above the units digit.

- **The program card coding indicates a left-zero field.**
- **The operator keys in the correct digits.**
- **The information is stored.**

Description

The program card is multi-punched with a 7, 8, and 9 (program 2) in the high-order position, for example column 40 (see Figure 1-10). The rest of the field is punched with 4's defining the field. The operator keys in the correct number of digits, then presses the dash key to start the punch-out including an 11 punch over the digit in the units position. *In our example,* we key-in one digit (5), and press the dash key to start punching.

Read-in Cycle 1: The machine is at a left-zero field, the program-select relay (308) is up. The 7, 8, and 9 starwheels energize the field 1, 2, and 3 relays (315, 324, 325), the field-size relays (209, 217, 226, 235, 216, 208, 218, 227), and the key-entry relay (304). The P-cam-gate relay (309) is up.

The operator presses the correct key, closing a latch contact. This energizes the correct relays in register 3A through the field-size relay points, the key-entry relay points, and the coding diodes. The punch clutch is energized through the key-entry relay and coding diodes. At 20° of the punch-clutch cycle, the keyboard is restored. The correct relays in register 3B are energized at 86°. This transfers the information from register 3A to register 3B. *In our example,* we stored a 5 in register 3B.

Circuit Objectives

1. Cycle 1 (store a 5):
   Close numeric-5 latch contact.
   Enter numeric information into register 3A and energize the punch clutch.
   Restore keyboard.
   Transfer register 3A to 3B.
   Retain information in register 3B.

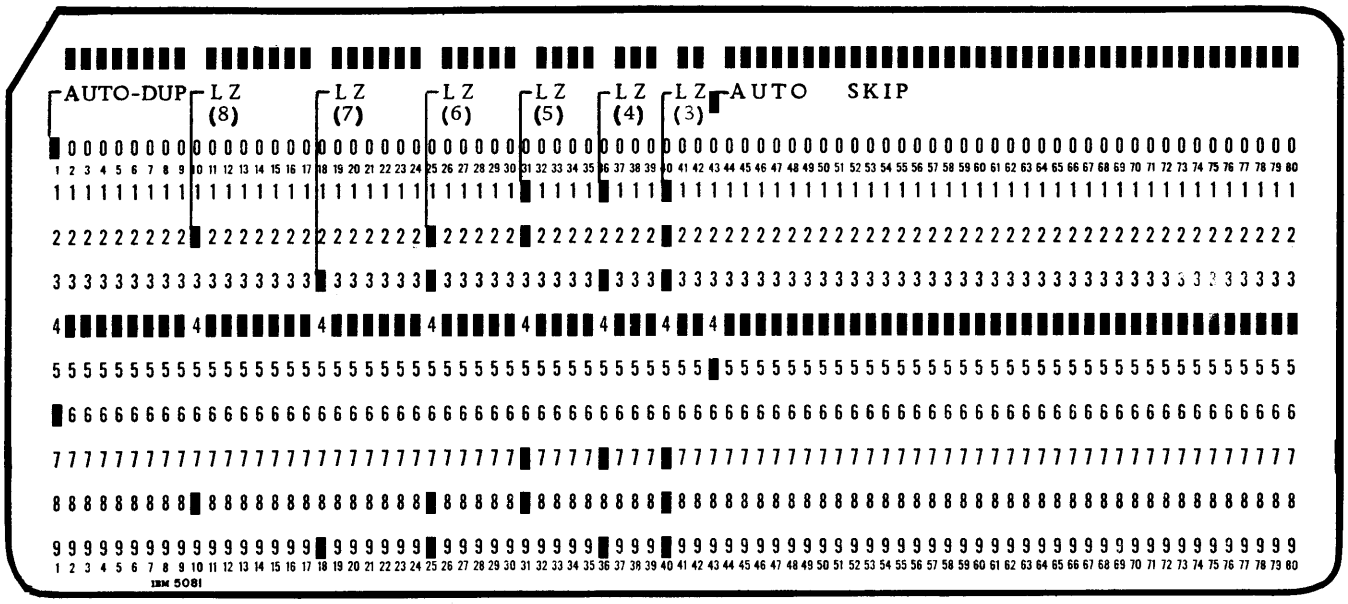


Figure 1-10. Left-Zero Program Card

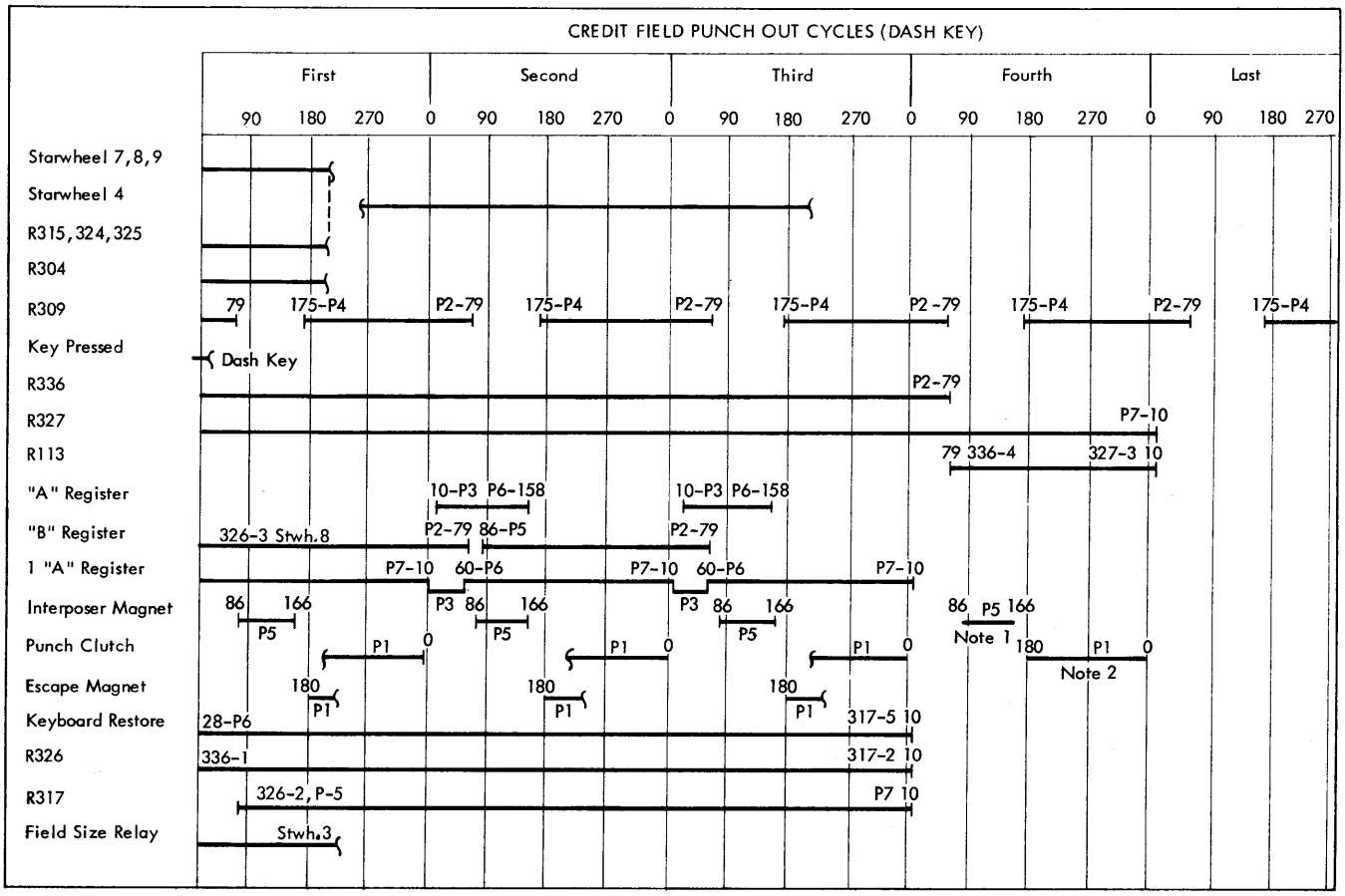
Credit Read-out, Punch-out

- **The operator presses the dash key for a credit field.**
- **The information is read out and punched.**
- **The units column is multi-punched.**

Description

The operator presses the dash key, energizing the necessary relays to start the read-out and punch-out, also relays to remember that it is a credit field. A dummy cycle must be taken first to read out the first digit to be punched. Each cycle will read out the next digit to be punched. When the end of the field is recognized, an extra cycle must be taken to punch the 11 punch. This cycle is a multi-punch cycle to prevent escapement from the units position of the field.

Read-out, Punch-out Cycle 1: Refer to Figure 1-11 for timing within cycles. The operator presses the dash key, closing the dash-latch contact. This energizes the credit-field 1 relay (336), read-out relay (326), and the punch clutch. As soon as the credit-field 1 relay (336) is up, the credit-field 2 relay (327) is energized through N/O points of credit-field 1 relay (336). The N/C 3-point of read-out relay (326) prevents the transfer of information from register to register.



Note 1 The 11 Interposer Magnet
Note 2 Punch Clutch Energized by Interpose Bail Contacts.

Figure 1-11. Punch-out Timing (3-Column Credit Field)

The information is held in the B-registers by P2, starwheel 2, and the N/O 5-point of read-out relay (326). The keyboard restore magnets are energized at 20° and are held energized for the rest of the punch-out cycles. The interposer magnet is energized at 86° through the N/O 6-point of the read-out relay (326), and the decode tree of register 1A relay points. The escape magnet is energized at 180° by P1 and interposer bail contacts. The escape-armature contact makes, energizing the escape-interlock relays. This allows the punch clutch to be energized for the next cycle. *In our example,* the interposer 0 magnet was energized, and an escapement to column 40 of the detail card occurred.

Read-out, Punch-out Cycle 2: During this cycle, the digit is punched that was set up during the last cycle. At 10° the B-registers transfer to the next A-registers. At 86° the A-registers transfer the information to the B-registers, and the interposer magnet is energized through the decode tree of register 1A relay points. The escape magnet is energized at 180°, the escape-armature contact makes, energizing the escape-interlock relays. The punch clutch is energized through points of the escape-interlock relays. *In our example,* a zero was punched in column 40, and the interposer 0 magnet was energized. The digit 5 transferred from register 3 to register 2. An escapement to column 41 of the detail card occurred.

Read-out, Punch-out Cycle 3: The digit is punched that was set up in last cycle. At 10° the B-registers transfer to the A-registers. The last keyed digit is in register 1A now. At 86° the interposer magnet is energized. At 180° the escape magnet is energized through the interposer bail contacts. The escape-armature contact makes, energizing the escape-interlock relays, allowing the punch clutch to be energized. During this escapement the starwheel 4 opens its circuit. *In our example,* the digit zero was punched in column 41, the interposer 5 magnet was energized, and an escapement to column 42 occurred.

Read-out, Punch-out Cycle 4: The last digit has been transferred from storage and is punched on this cycle. At 10°, the punch-out relay (317) is dropped). The opening of the punch-out relay N/O points drop the read-out 1 relay (326). At 79° (P2) credit-field 1 relay (336) drops. The multi-punch relay (113) is energized through the N/O 3-point of the credit-field 2 relay (327), and the N/C 3-point of the credit field 1 relay (326). This prevents a circuit to the escape magnet when the interposer 11 magnet is energized at 86° (P5) through the N/C 3-point of the credit-field 1 relay (336) and the N/O 2-point of the credit-field 2 relay (327). The punch clutch is energized through the N/O 6-point of the multi-punch relay (113) and the interposer bail contacts. *In our example,* a 5 was punched in column 42, and the interposer 11 magnet was energized.

Read-out, Punch-out Cycle 5: The credit 11 is punched during this cycle. At 10° (P7), the credit-field 2 relay (327) is dropped. The N/O 3-point of the credit-field 2 relay (327) opens the circuit to the multi-punch relay (113). The punch clutch latches at 345°. *In our example,* the 11 punch is punched above the 5 punched in column 42.

Circuit Objectives

1. Cycle 1 (energize interposer 0 for punching in next cycle):
   Close dash-latch contact.
   Energize credit-field 1 relay and punch clutch.
   Energize credit-field 2 relay, read-out 1 and 2 relays.
   Prevent transfer of information in registers.
   Provide hold on the B-registers and register 1A.
   Provide a continuous hold on restore magnets.
   Energize interposer 0 magnet.
   Energize the punch-out relay.
   Provide hold to the field 1, 2, and 3 relays.
   Drop key-entry relay.
   Energize escape magnet.
   Energize escape-interlock relays.
   Energize punch clutch.

2. Cycle 2 (punch a 0, energize interposer 0 magnet):
   Transfer B-registers to next A-registers.
   Hold 1A register until 10° of next cycle.
   Transfer A-registers to B-registers.
   Hold B-register information until next cycle.
   Energize interposer 0 magnet.
   Energize escape magnet.
   Energize escape-interlock relays.
   Energize punch clutch.

3. Cycle 3 (punch a 0, energize interposer-5 magnet):
   Transfer B-registers to next A-registers.
   Hold register 1A information until 10° next cycle.
   Transfer A-registers to B-registers.
   Energize interposer 5 magnet.
   Energize escape magnet.
   Energize escape-interlock relays.
   Energize punch clutch.
   Break starwheel 4 contact.

4. Cycle 4 (punch a 5, energize interposer 11 magnet):
   Drop punch-out relay.
   Drop read-out relays and field 1, 2, and 3 relays.
   Open circuit to keyboard-restore magnets.

Drop credit-field 1 relay.
Energize the multi-punch relay.
Prevent energizing the escape magnet.
Energize interposer 11 magnet.
Energize the punch clutch.

5. Cycle 5 (punch an 11 above the 5):
   Drop credit-field 2 relay.
   Drop multi-punch relay.

Left-Zero Logic Controls

Figure 1-12 is a diagram of the basic left-zero operations and their controls. The read-in operations are shown with connecting solid lines, and the read-out operations are shown with broken lines. The diagram can be used for both troubleshooting and a quick reference to general operation.

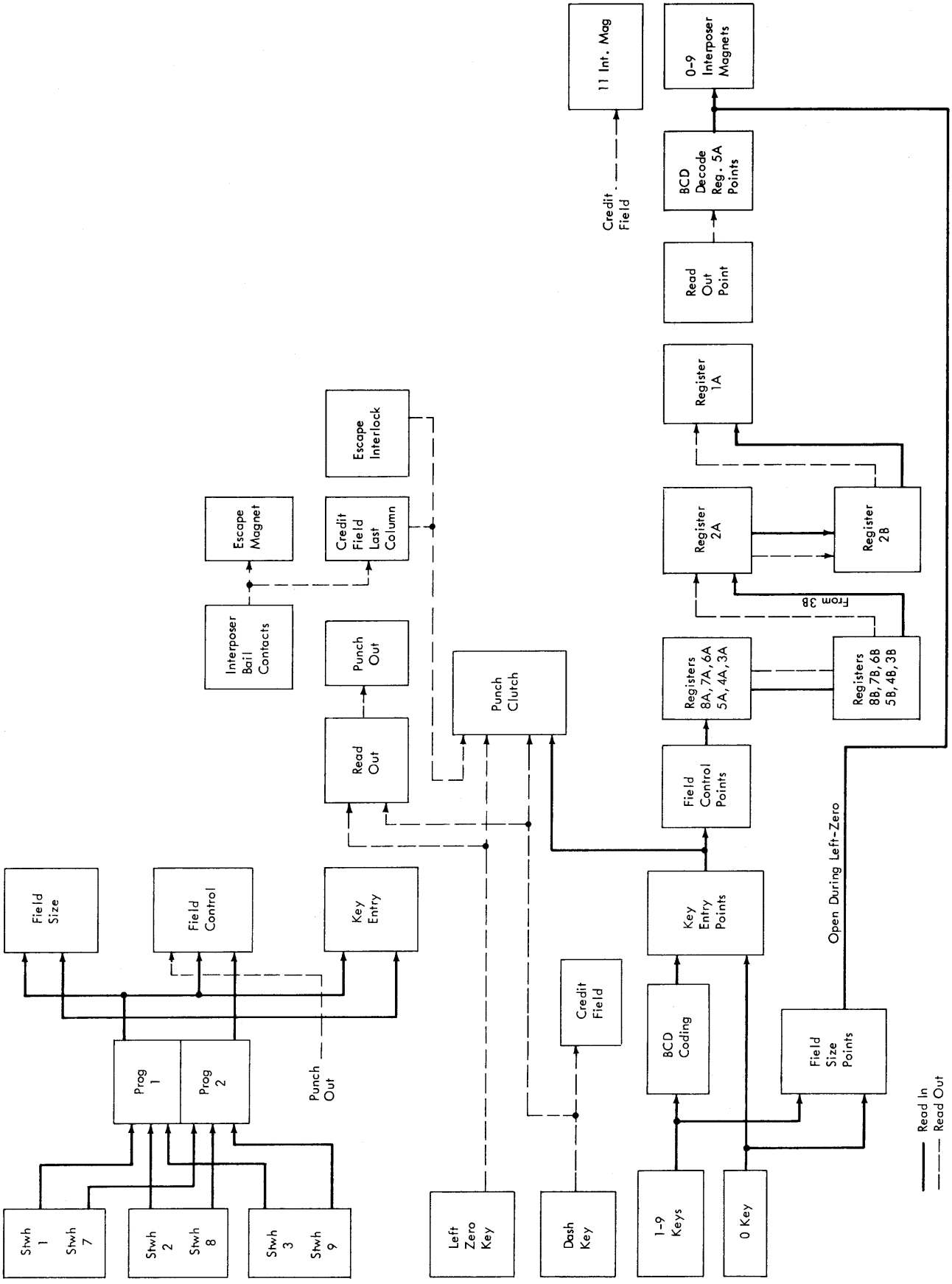


Figure 1-12. Left-Zero Logic Controls and Flow

Purpose of Left-Zero Relays and Points

Relay	*Point*	*Type*	*Purpose*
201A			Register 3A, 1-bit relay.
	1	N/O	Hold circuit to relay 201A.
	2	N/O	Pick circuit to relay 201B.
201B			Register 3B, 1-bit relay.
	1	N/O	Hold circuit to relay 201B.
	2	N/O	Pick circuit to relay 328A.
202A			Register 4A, 1-bit relay.
	1	N/O	Hold circuit to relay 202A.
	2	N/O	Pick circuit to relay 202B.
202B			Register 4B, 1-bit relay.
	1	N/O	Hold circuit to relay 202B.
	2	N/O	Pick circuit to relay 201A.
203A			Register 5A, 1-bit relay.
	1	N/O	Hold circuit to relay 203A.
	2	N/O	Pick circuit to relay 203B.
203B			Register 5B, 1-bit relay.
	1	N/O	Hold circuit to relay 203B.
	2	N/O	Pick circuit to relay 202A.
204A			Register 6A, 1-bit relay.
	1	N/O	Hold circuit to relay 204A.
	2	N/O	Pick circuit to relay 204B.
204B			Register 6B, 1-bit relay.
	1	N/O	Hold circuit to relay 204B.
	2	N/O	Pick circuit to relay 203A.
205A			Register 7A, 1-bit relay.
	1	N/O	Hold circuit to relay 205A.
	2	N/O	Pick circuit to relay 205B.
205B			Register 7B, 1-bit relay.
	1	N/O	Hold circuit to relay 205B.
	2	N/O	Pick circuit to relay 204A.
206A			Register 8A, 1-bit relay.
	1	N/O	Hold circuit to relay 206A.
	2	N/O	Pick circuit to relay 206B.
206B			Register 8B, 1-bit relay.
	1	N/O	Hold circuit to relay 206B.
	2	N/O	Pick circuit to relay 205A.
208			Field-Size relay, BCD coding circuits to A-registers.
	1	N/C	4-bit input to register 7A.
	2	N/C	8-bit input to register 7A.
	3	N/C	1-bit input to register 6A.
	4	N/C	2-bit input to register 6A.
	5	N/C	8-bit input to register 6A.
	6	N/C	4-bit input to register 6A.
209			Field-Size relay, BCD coding to the A-registers.
	1	N/O	Circuit for 8-bit.
	2	N/O	Circuit for 4-bit.
210A			Register 3A, 2-bit relay.
	1	N/O	Hold circuit to relay 210A.
	2	N/O	Pick circuit to relay 210B.
210B			Register 3B, 2-bit relay.
	1	N/O	Hold circuit to relay 210B.
	2	N/O	Pick circuit to relay 310A.
211A			Register 4A, 2-bit relay.
	1	N/O	Hold circuit to relay 211A.
	2	N/O	Pick circiut to relay 211B.
211B			Register 4B, 2-bit relay.
	1	N/O	Hold circuit to relay 211B.
	2	N/O	Pick circuit to relay 210A.
212A			Register 5A, 2-bit relay.
	1	N/O	Hold circuit to relay 212A.
	2	N/O	Pick circuit to relay 212B.
212B			Register 5B, 2-bit relay.
	1	N/O	Hold circuits to relay 212B.
	2	N/O	Pick circuit to relay 211A.
213A			Register 6A, 2-bit relay.
	1	N/O	Hold circuit to relay 213A.
	2	N/O	Pick circuit to relay 213B.
213B			Register 6B, 2-bit relay.
	1	N/O	Hold circuit to relay 213B.
	2	N/O	Pick circuit to relay 212A.
214A			Register 7A, 2-bit relay.
	1	N/O	Hold circuit to relay 214A.
	2	N/O	Pick circuit to relay 214B.
214B			Register 7B, 2-bit relay.
	1	N/O	Hold circuit to relay 214B.
	2	N/O	Pick circuit to relay 213A.
215A			Register 8A, 2-bit relay.
	1	N/O	Hold circuit to relay 215A.
	2	N/O	Pick circuit to relay 215B.
215B			Register 8B, 2-bit relay.
	1	N/O	Hold circuit to relay 215B.
	2	N/O	Pick circuit to relay 214A.
216			Field-Size relay, BCD coding to the A-registers.
	1	N/O	4-bit input to register 4A.
	2	N/O	8-bit input to register 4A.
	3	N/O	1-bit input to register 3A.
	4	N/O	2-bit input to register 3A.
	5	N/O	5-bit input to register 3A.
	6	N/O	8-bit input to register 3A.
217			Field-Size relay, BCD coding to the A-registers.
	1	N/O	Circuit for 2-bit.
	2	N/O	Circuit for 4-bit.
	3	N/O	Circuit for 8-bit.
	4	N/O	Circuit for 2-bit.
	5	N/O	Circuit for 1-bit.
	6	N/O	Circuit for 1-bit.
218			Field-Size relay, BCD coding to the A-registers.
	1	N/O	Circuit for 4-bit.
	2	N/O	Circuit for 8-bit.
219A			Register 3A, 4-bit relay.
	1	N/O	Hold circuit for relay 219A.
	2	N/O	Pick circuit for relay 219B.
219B			Register 3B, 4-bit relay.
	1	N/O	Hold circuit to relay 219B.
	2	N/O	Pick circuit to relay 310A.

Relay	Point	Type	Purpose
220A			Register 4A, 4-bit relay.
	1	N/O	Hold circuit to relay 220A.
	2	N/O	Pick circuit to relay 220B.
220B			Register 4B, 4-bit relay.
	1	N/O	Hold circuit to relay 220B.
	2	N/O	Pick circuit to relay 219A.
221A			Register 5A, 4-bit relay.
	1	N/O	Hold circuit to relay 221A.
	2	N/O	Pick circuit to relay 221B.
221B			Register 5B, 4-bit relay.
	1	N/O	Hold circuit to relay 221B.
	2	N/O	Pick circuit to relay 220A.
222A			Register 6A, 4-bit relay.
	1	N/O	Hold circuit to relay 222A.
	2	N/O	Pick circuit to relay 222B.
222B			Register 6B, 4-bit relay.
	1	N/O	Hold circuit to relay 222B.
	2	N/O	Pick circuit to relay 221A.
223A			Register 7A, 4-bit relay.
	1	N/O	Hold circuit to relay 223A.
	2	N/O	Pick circuit to relay 223B.
223B			Register 7B, 4-bit relay.
	1	N/O	Hold circuit to relay 223B.
	2	N/O	Pick circuit to relay 222A.
224A			Register 8A, 4-bit relay.
	1	N/O	Hold circuit to relay 224A.
	2	N/O	Pick circuit to relay 224B.
224B			Register 8B, 4-bit relay.
	1	N/O	Hold circuit to relay 224B.
	2	N/O	Pick circuit to relay 223A.
226			Field-Size relay, BCD coding to the A-registers.
	1	N/C	1-bit input to register 8A.
	2	N/C	2-bit input to register 8A.
	3	N/C	4-bit input to register 8A.
	4	N/C	8-bit input to register 8A.
	5	N/C	2-bit input to register 7A.
	6	N/C	2-bit input to register 7A.
227			Field-Size relay, BCD coding to the A-registers.
	1	N/O	Circuit for 1-bit.
	2	N/C	Circuit for 1-bit.
	3	N/C	Circuit for 2-bit.
	4	N/C	Circuit for 4-bit.
	5	N/C	Circuit for 8-bit.
	6	N/O	Circuit for 2-bit.
228A			Register 3A, 8-bit relay.
	1	N/O	Hold circuit to relay 228A.
	2	N/O	Pick circuit to relay 228B.
228B			Register 3B, 8-bit relay.
	1	N/O	Hold circuit to relay 228B.
	2	N/O	Pick circuit to relay 301A.
229A			Register 4A, 8-bit relay.
	1	N/O	Hold circuit to relay 229A.
	2	N/O	Pick circuit to relay 229B.
230A			Register 5A, 8-bit relay.
	1	N/O	Hold circuit to relay 230A.
	2	N/O	Pick circuit to relay 230B.
230B			Register 5B, 8-bit relay.
	1	N/O	Hold circuit to relay 230B.
	2	N/O	Pick circuit to relay 229A.
231A			Register 6A, 8-bit relay.
	1	N/O	Hold circuit to relay 231A.
	2	N/O	Pick circuit to relay 231B.
231B			Register 6B, 8-bit relay.
	1	N/O	Hold circuit to relay 231B.
	2	N/O	Pick circuit to relay 230A.
232A			Register 7A, 8-bit relay.
	1	N/O	Hold circuit to relay 232A.
	2	N/O	Pick circuit to relay 232B.
232B			Register 7B, 8-bit relay.
	1	N/O	Hold circuit to relay 232B.
	2	N/O	Pick circuit to relay 231A.
233A			Register 8A, 8-bit relay.
	1	N/O	Hold circuit to relay 233A.
	2	N/O	Pick circuit to relay 233B.
233B			Register 8B, 8-bit relay.
	1	N/O	Hold circuit to relay 233B.
	2	N/O	Pick circuit to relay 232A.
235			Field-Size relay, BCD coding to A-register.
	1	N/O	2-bit input to register 5A.
	2	N/O	1-bit input to register 5A.
	3	N/O	4-bit input to register 5A.
	4	N/O	8-bit input to register 5A.
	5	N/O	1-bit input to register 4A.
	6	N/O	2-bit input to register 4A.
301A			Register 2A, 8-bit relay.
	1	N/O	Hold circuit for relay 301A.
	2	N/O	Pick circuit for relay 301B.
301B			Register 2B, 8-bit relay.
	1	N/O	Hold circuit for relay 301B.
	2	N/O	Pick circuit for relay 329.
304			Key entry allows the keyed information to enter the field-size relays.
	1	N/O	Circuit to the keyboard-restore magnets.
	2	N/O	Circuit energize the punch clutch when a zero is keyed.
	3	N/O	Circuit from BCD coding network to the field-size relays for an 8-bit.
	4	N/O	Circuit from BCD coding network to the field-size relays for a 1-bit.
	5	N/O	Circuit from BCD coding network to the field-size relays for a 4-bit.
	6	N/O	Circuit from BCD coding network to the field-size relays for a 2-bit.
308			Program select, picked while in program 2.
	1	N/O	Circuit from starwheel 9.
	2	N/C	Circuit from starwheel 3.
	3	N/C	Circuit from starwheel 2.
	4	N/O	Circuit from starwheel 8.
309			P-cam-gate, circuits from P-CB's when needed. Prevents any extra pulses due to bounce of CB.
	1	N/O	Circuit from P2 to hold relay 209 up until P2 breaks.
	2	N/C	Gates P5 to the B-registers relays.
	3	N/C	
	4	N/O	Gates P3 to the A-registers relays.
310A			Register 2A, 4-bit relay.
	1	N/O	Hold circuit for relay 310A.
	2	N/O	Pick circuit for relay 310B.
310B			Register 2B, 4-bit relay.
	1	N/O	Hold circuit for relay 310B.
	2	N/O	Pick circuit for register 1A, 8-bit relay (329).

Relay	Point	Type	Purpose
311			Register 1A, 4-bit relay (1 of 2)
	1	N/O	Circuit to the interposer 5 magnet out of the BCD decode tree.
	2	N/C	Circuit to the interposer 3 magnet out of the BCD decode tree.
	3	N/C	Circuit to the interposer 2 magnet out of the BCD decode tree.
	4	N/O	Circuit to the interposer 7 magnet out of the BCD decode tree.
315			Field-1 relay, controls circuit to interposer magnets from the keyboard.
	1	N/C	Circuit to interposer 9 magnet from keyboard.
	2	N/C	Circuit to interposer 8 magnet from keyboard.
	3	N/C	Circuit to interposer 7 magnet from keyboard.
	4	N/C	Circuit to interposer 6 magnet from keyboard.
	5	N/C	Circuit to interposer 5 magnet from keyboard.
	6	N/C	Circuit to interposer 4 magnet from keyboard.
317			Punch-out relay controls circuits during punch-out time of the left-zero operation.
	1	N/O	Hold circuit for relay 317.
	2	N/O	Hold circuit for the read-out relays, credit-field 1 relay.
	4	N/C	Hold circuit for register 1A during part of the first read-out cycle.
	5	N/O	Circuit to hold the keyboard restored during punch-out.
	6	N/O	Circuit for P3 to the A-registers after the first read-out cycle.
319			Register 2A, 2-bit relay.
	1	N/O	Hold circuit for relay 319A.
	2	N/O	Pick circuit for relay 319B.
319B			Register 2B, 2-bit relay.
	1	N/O	Hold circuit for relay 319B.
	2	N/O	Pick circuit to register 1A, 2-bit relay.
320			Register 1A, 4-bit relay (1 of 2).
	1	N/O	Hold circuit to register 1A, 4-bit relays.
	2	N/O	Circuit to the interposer 6 magnet out of the BCD decode tree.
	3	N/C	Circuit to the interposer 1 magnet out of the BCD decode tree.
	4	N/C	Circuit to the interposer 0 magnet out of the BCD decode tree.
	5	N/O	
	6	N/O	Circuit to the interposer 4 magnet out of the BCD decode tree.
321			Register 1A, 2-bit relay.
	1	N/O	Hold circuit for relay 321.
	2	N/O	Circuit for 2-bit decode for a 2 or 6.
	3	N/C	Circuit for 2-bit decode for a 1 or 5.
	4	N/C	Circuit for 2-bit decode for a 0 or 4.
	5	N/O	
	6	N/O	Circuit for 2-bit decode for a 3 or 7.
324			Field-2 relay, controls circuits to interposer magnets from the keyboard.
	1	N/C	Circuit to interposer 3 magnet from keyboard.
	2	N/C	Circuit to interposer 2 magnet from keyboard.
	3	N/C	Circuit to interposer 1 magnet from keyboard.
	4	N/C	Circuit to interposer 0 magnet from keyboard.
	5	N/C	Circuit to interposer 11 magnet from keyboard.
	6	N/C	Circuit to alpha-relay from starwheel 1 and 7.
325			Field-3 relay, controls the digit-11 line from the keyboard to the left-zero relays.
	1	N/O	Circuit to pick the punch clutch and the credit-field 1 relay.
326			Read-out relay, controls circuit during read-out time of a left-zero field.
	1	N/O	Hold circuit to the read-out relay and credit-field 1 relay.
	2	N/O	Pick circuit to the punch-out relay.
	3	N/C	Prevents P3 pulse to the A-register during the first read-out cycle of a left-zero field.
	4	N/C	Pick circuit to multi-punch relay during credit punching.
	5	N/O	Hold circuit to the B-registers during the first part of the first read-out cycle.
	6	N/O	Circuit to the BCD decode tree from P5.
327			Credit-Field 2 relay, set up circuits to energize the interposer 11 magnet at the units position of the field.
	1	N/O	Hold circuit to relay 327.
	2	N/O	Circuit to energize the interposer 11 magnet.
	3	N/O	Circuit to energize the multi-punch relay.
	4	N/O	
328A			Register 2A, 1-bit relay.
	1	N/O	Hold circuit to relay 328A.
	2	N/O	Pick circuit to relay 328B.
328B			Register 2B, 1-bit relay.
	1	N/O	Hold circuit to relay 328B.
	2	N/O	Pick circuit to register 1A, 1-bit relay (330).
329			Register 1A, 8-bit relay.
	1	N/O	Hold circuit to relay 329.
	2	N/O	
	3	N/O	Circuit for 8-bit decode for a 0.
	4	N/O	Circuit for 8-bit decode for an 8 or 9.
330			Register 1A, 1-bit relay.
	1	N/O	Hold circuit to relay 330.
	2	N/O	Circuit to the interposer 9 magnet out of the BCD decode tree.
	3	N/C	Circuit for 1-bit decode for a 0, 2, 4, and 6.
	4	N/C	Circuit to the interposer 8 magnet out of the BCD decode tree.
	5	N/O	
	6	N/O	Circuit for 1-bit decode for a 1, 3, 5, and 7.

Relay	*Point*	*Type*	*Purpose*
336			Credit-Field 1 relay, set up circuits to punch an 11 punch in the units position of a credit field.
	1	N/O	Pick circuit to relay 327.
	2	N/O	Prevents dup 2 relay from picking before the credit punch operation begins.
	3	N/C	Circuit to energize interposer 11 magnets in units position of a credit-left-zero field.
	4	N/C	
	5	N/O	
	6	N/O	Hold circuit to relay 236 until P2 breaks.

Instructional Wiring Diagram

The following diagrams are to be used only for instructional purposes.

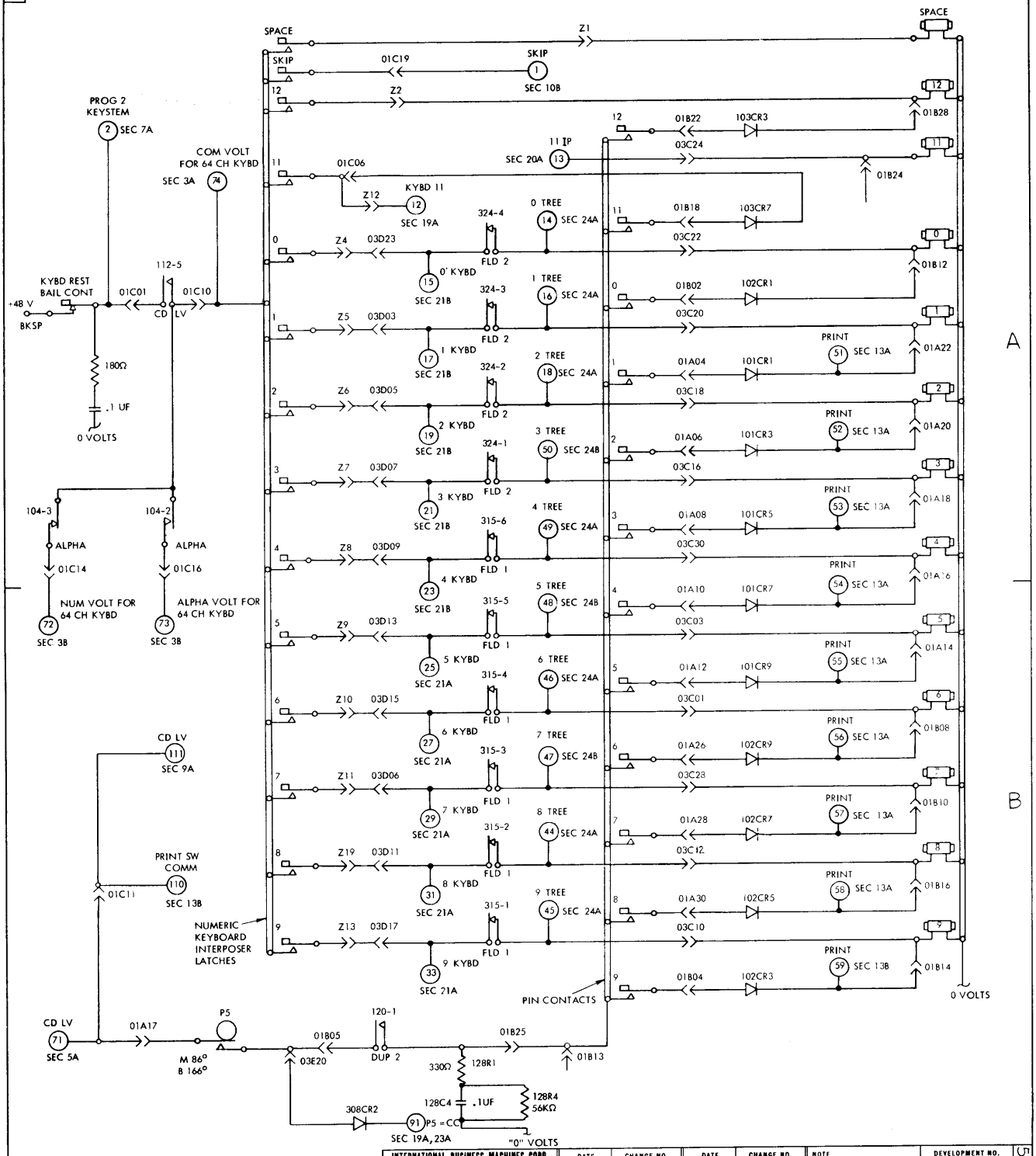
5393433

01.29.01.1

NUMERIC KEYBOARD AND INTERPOSERS

(FOR INSTRUCTIONAL USE ONLY)

LEFT ZERO



NOTES:

XI POINT TO POINT WIRING FOR +48 AND "0" VOLT NET SHOWN ON 01.29.16.0

SIMILAR TO 5373553, 5373564

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE X PRINT TO ENG. SPEC. NO.	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM 01.29.01.1							895291	
DESIGN		MODEL							
DETAIL									01.29.01.1
CHECK		DRAW							
APPRO		CHECK							

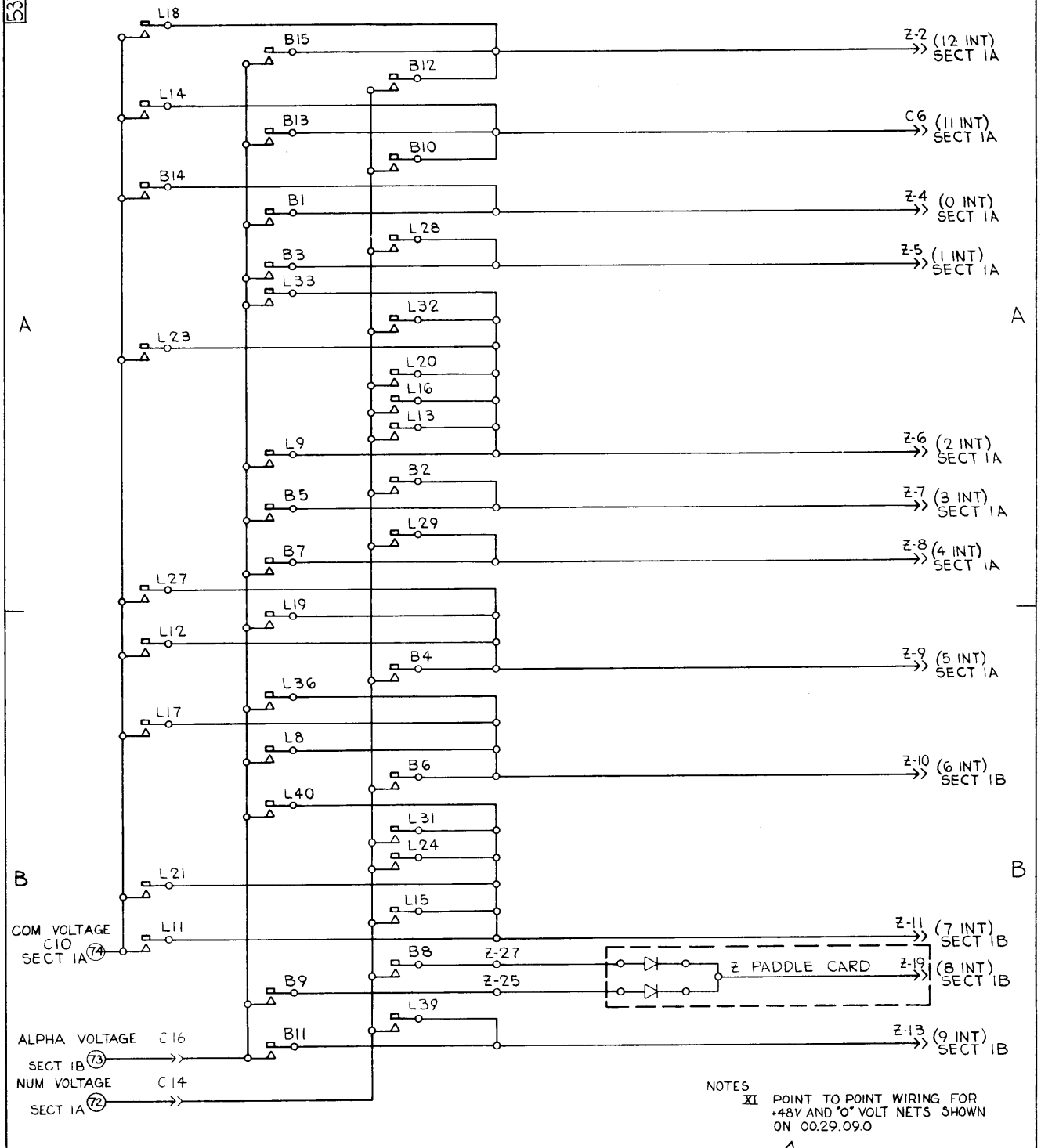
5393433

5373554

00.29.03.1

64 CHARACTER KYBD

(FOR INSTRUCTIONAL USE ONLY)



NOTES

XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 00.29.09.0

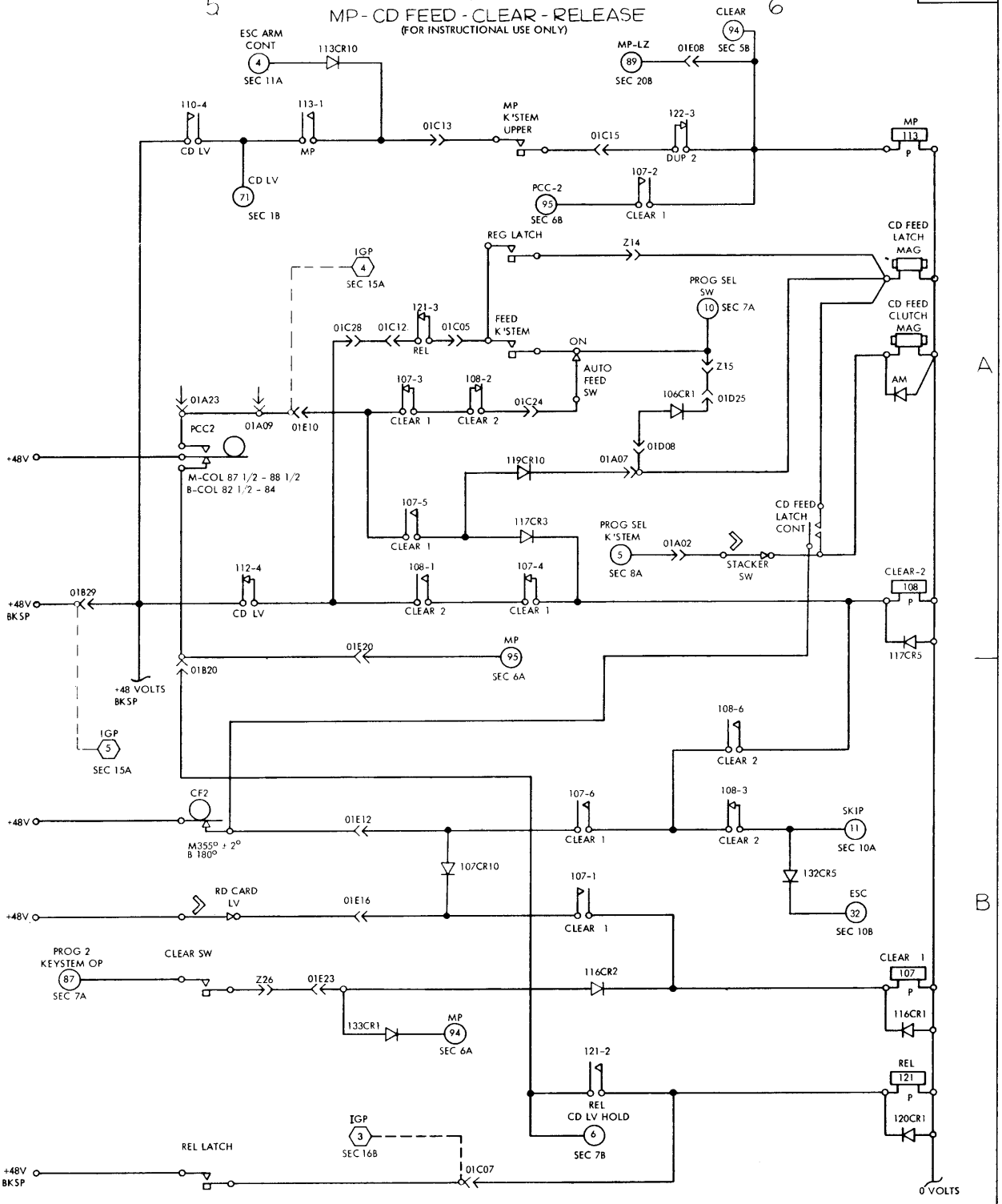
INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SYSTEMS DIAGRAM 00.29.03.1					X PRINT TO ENG. SPEC. NO. 895291	
DESIGN MODEL						
DETAIL						
CHECK DRAW						00.29.03.1
APPRO CHECK						

5373554

5 6

MP - CD FEED - CLEAR - RELEASE

(FOR INSTRUCTIONAL USE ONLY)



NOTES:

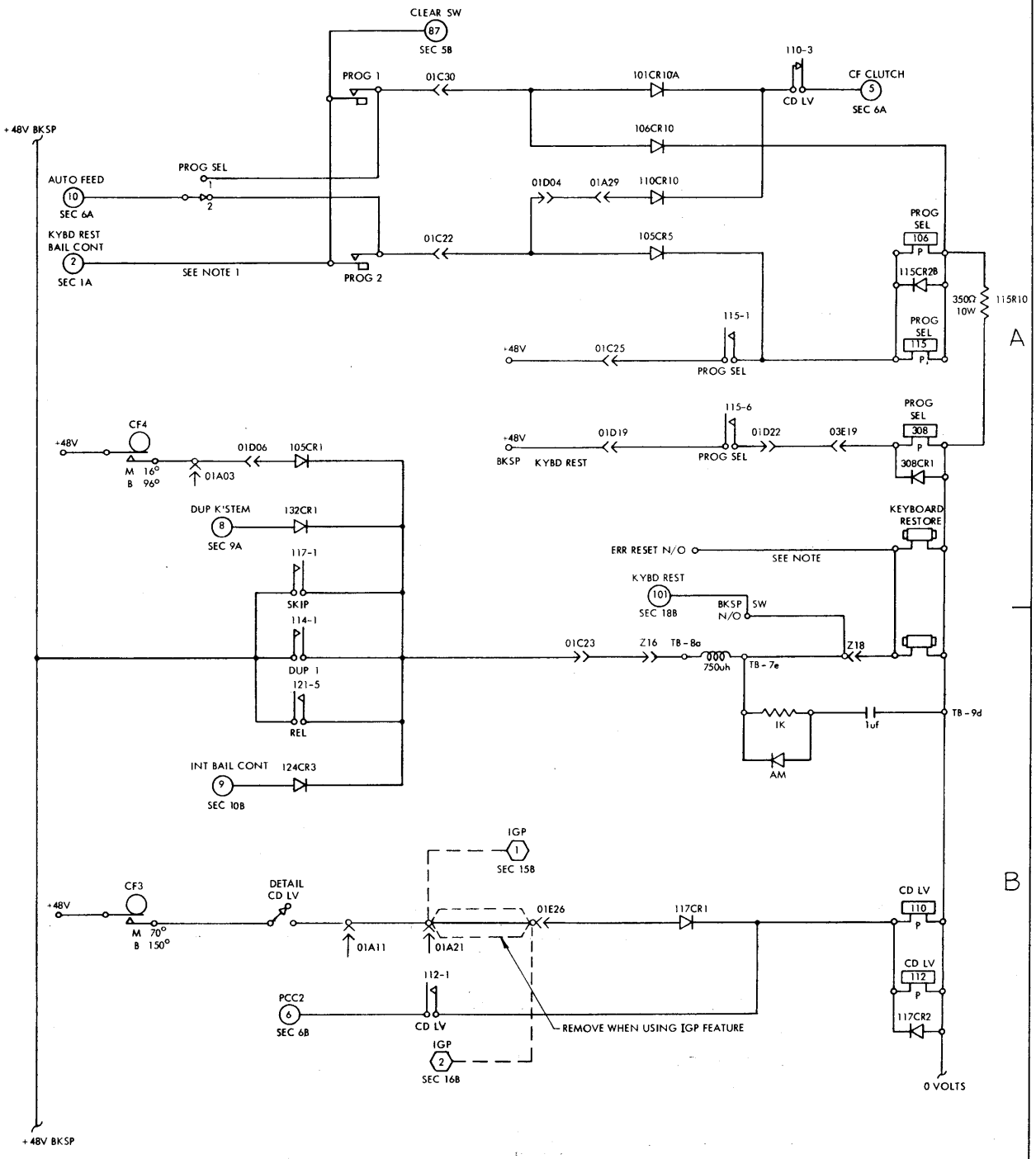
XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

SIMILAR TO 5373555, 5373562

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM 01.29.02.1							X PRINT TO ENG. SPEC. NO. 895291	
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.02.1
APPRO		CHECK							

KEYBOARD RESTORE - PROG SEL - CD LV

(FOR INSTRUCTIONAL USE ONLY)



NOTES:

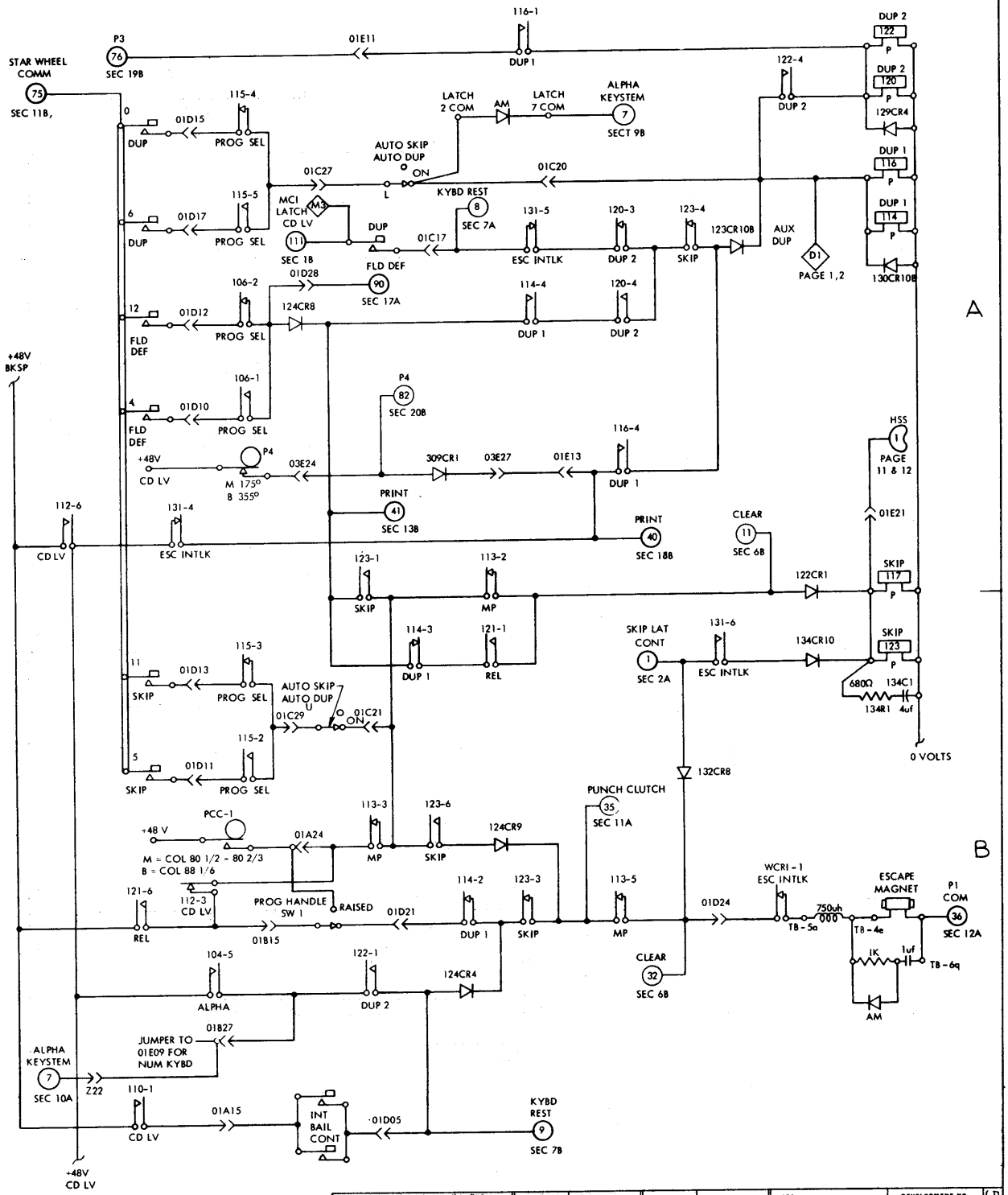
X1 POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

SIMILAR TO 5373556, 5373563

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEM DIAGRAM							X PRINT TO ENG. SPEC. NO.	
	01.29.03.1							895291	
DESIGN		MODEL							
DETAIL									
CHECK		C-HAW							01.29.03.1
APPRO		CHECK							

DUP - ESCAPE - SKIP

(FOR INSTRUCTIONAL USE ONLY)



NOTES:

XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

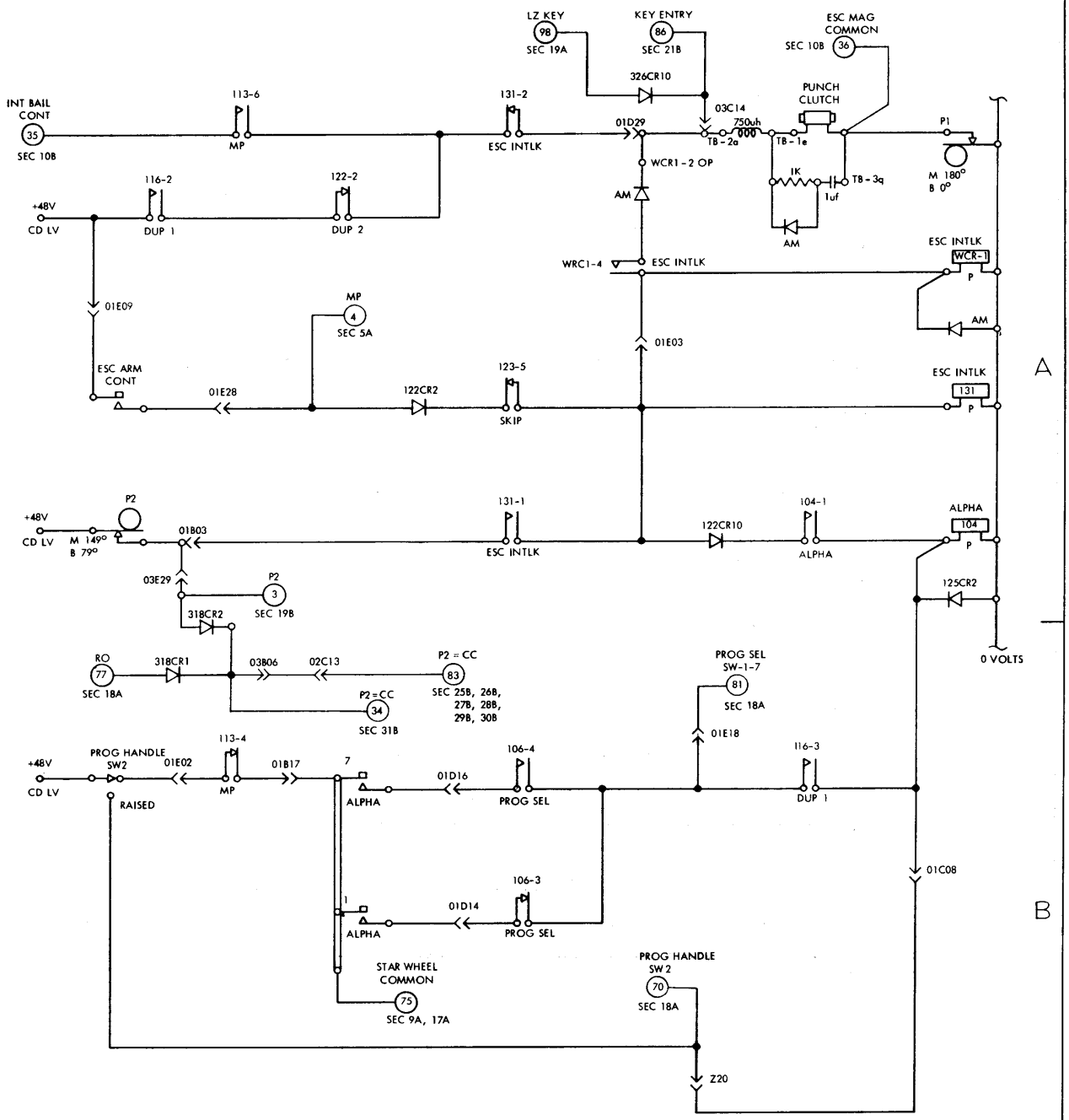
SIMILAR TO 5373557

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.04.1								
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.04.1
APPRO		CHECK							

11 12

PUNCH CLUTCH - ESC INTLK - ALPHA

(FOR INSTRUCTIONAL USE ONLY)



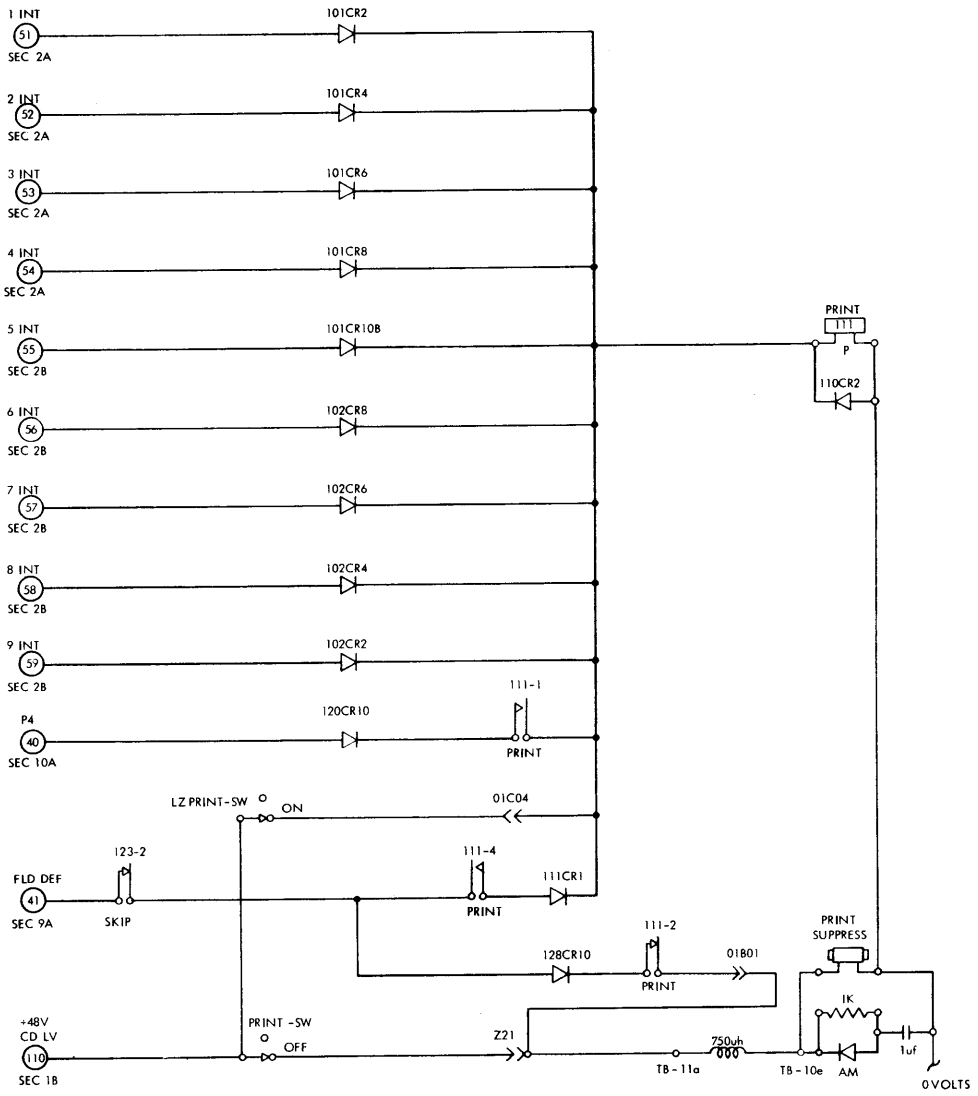
NOTES:

XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

SIMILAR TO 5373558

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.05.1								
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							
APPRO		CHECK							

PRINT
(FOR INSTRUCTIONAL USE ONLY)



NOTES:
XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

SIMILAR TO 5373559

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.06.1								
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.06.1
APPRO		CHECK							

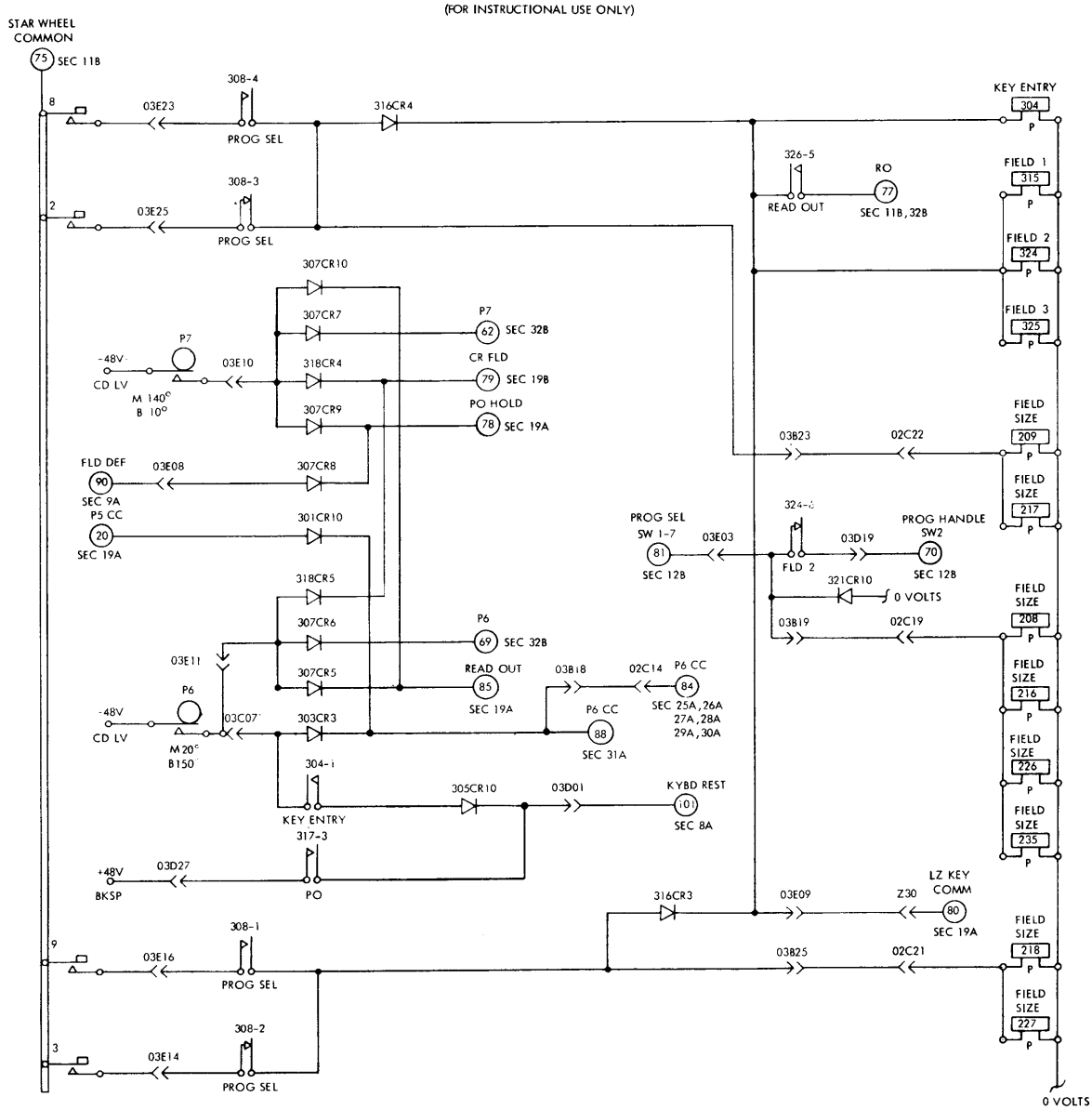
SECTIONS 15 and 16

The wiring diagram page for the Intersperse Gang Punch Feature is shown in Sections 15-16.

Order part number 5404077 for machines having this special feature.

KEY ENTRY - FIELD SIZE

(FOR INSTRUCTIONAL USE ONLY)



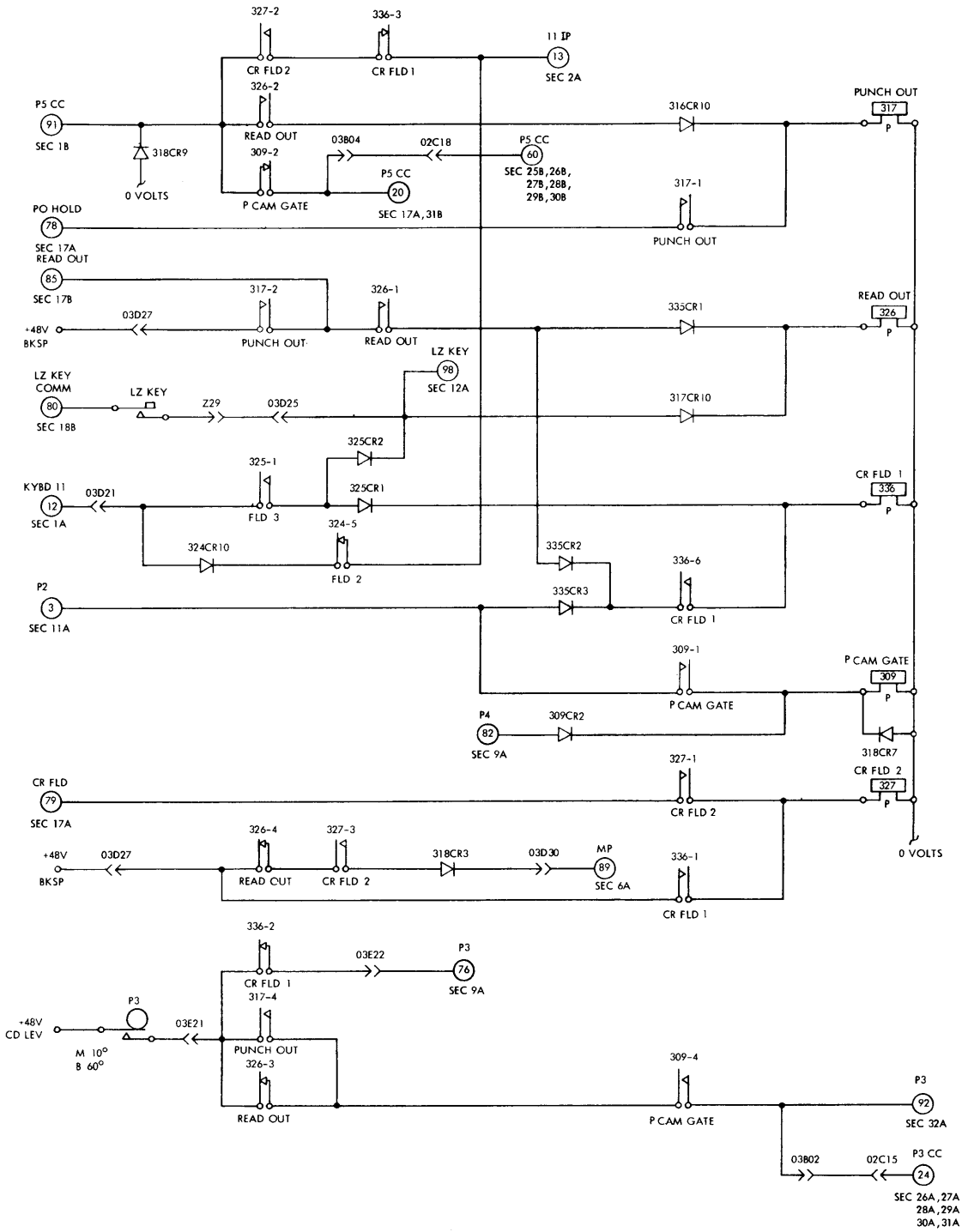
NOTES:

XI POINT TO POINT WIRING FOR +48V AND '0' VOLT NETS SHOWN ON 01.29.16.0

INTERNATIONAL BUSINESS MACHINES CORP.			DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM						X PRINT TO ENG. SPEC. NO. 895291	
	01.29.07.1							
DESIGN		MODEL						
DETAIL								
CHECK		DRAW						01.29.07.1
APPRO		CHECK						

PUNCH OUT-READ OUT-CREDIT FIELD

(FOR INSTRUCTIONAL USE ONLY)



A

B

NOTES:

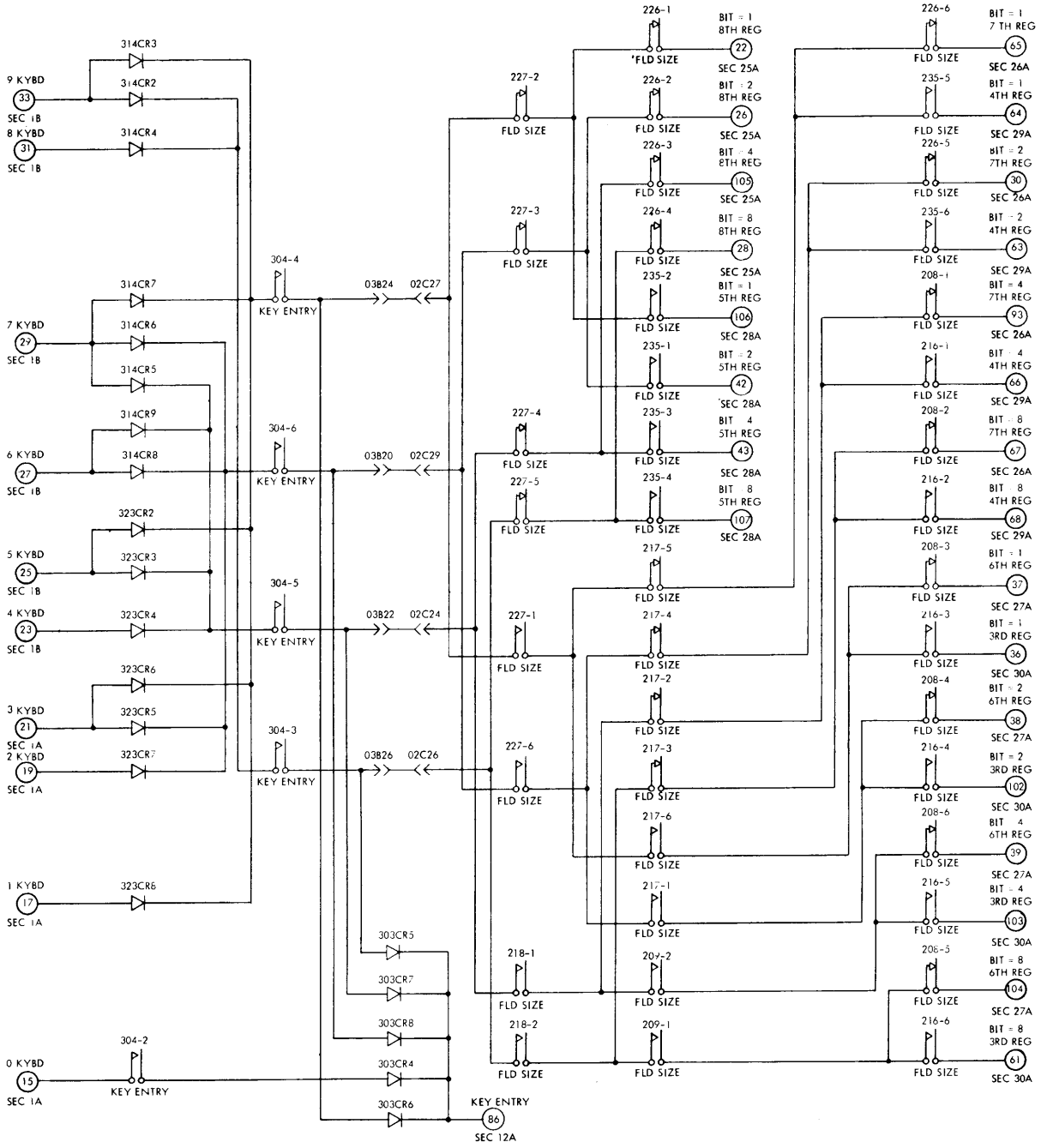
XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SYSTEMS DIAGRAM								X PRINT TO ENG. SPEC. NO.	
01.29.08.1								895291	
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.08.1
APPRO		CHECK							

21 22

FIELD SIZE

(FOR INSTRUCTIONAL USE ONLY)



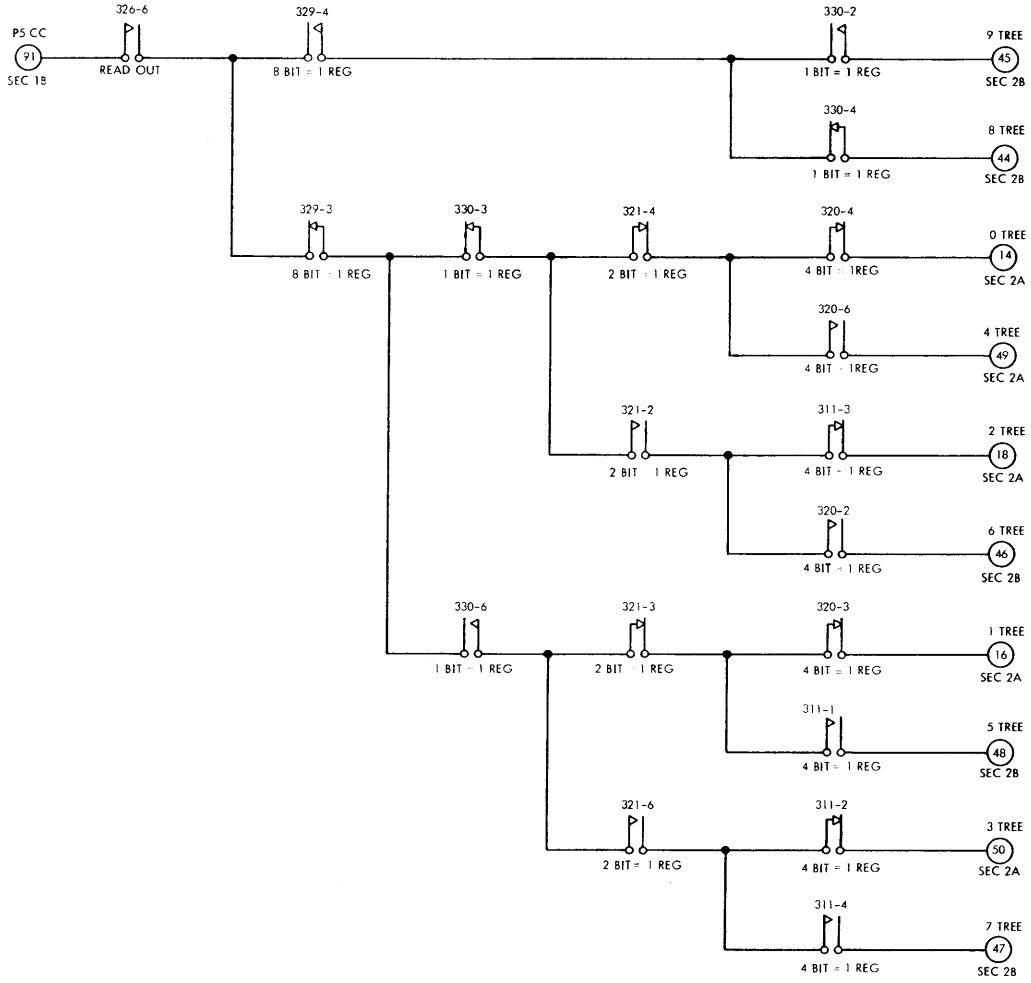
NOTES:

XI POINT TO POINT WIRING FOR +48V AND "0" VOLT NETS SHOWN ON 01.29.16.0

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO.	
	01.29.09.1							895291	
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.09.1
APPRO		CHECK							

TREE

(FOR INSTRUCTIONAL USE ONLY)



A

B

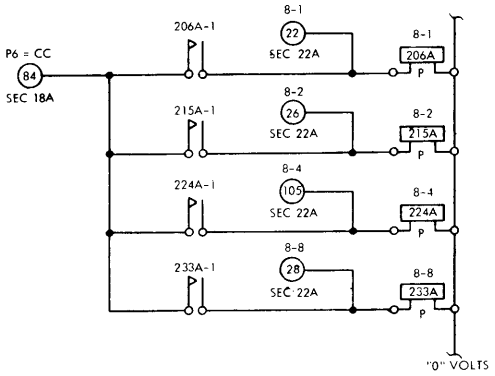
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYS EMS DIAGRAM							X PRINT TO ENG. SPEC. NO.	
	01.29.01.1							895291	
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.10.1
APPRO		CHECK							

5393443

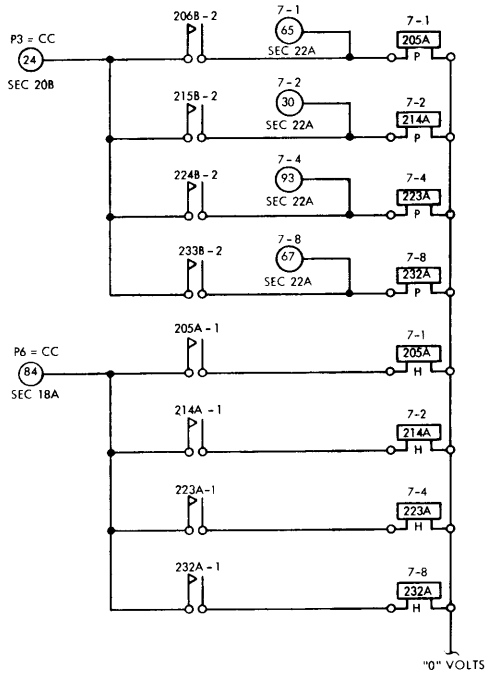
01.29.11.1

(FOR INSTRUCTIONAL USE ONLY)

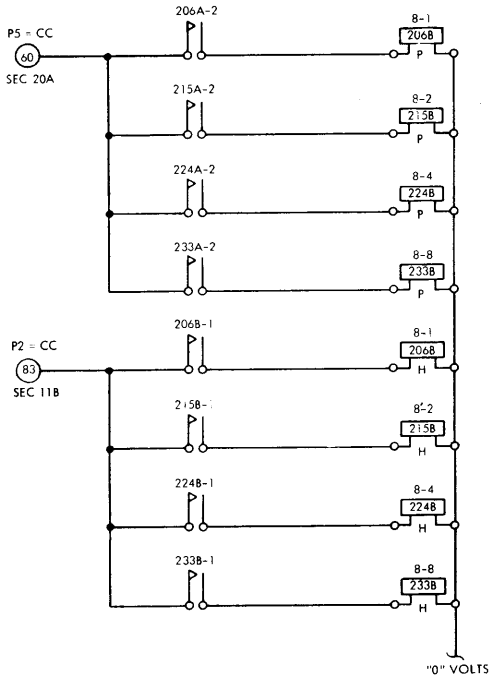
25
8TH REGISTER

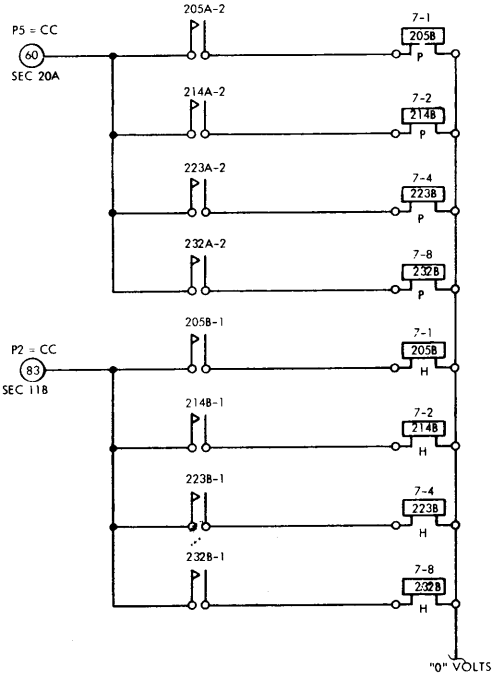


26
7TH REGISTER



A





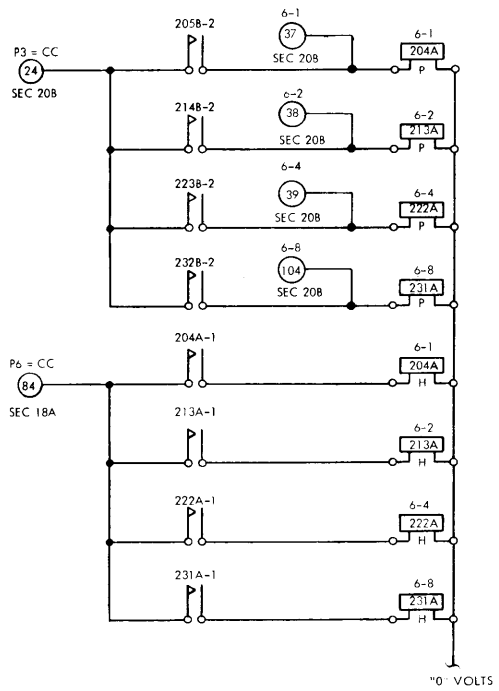
B

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO.	
	01.29.11.1							895291	
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.11.1
APPRO		CHECK							

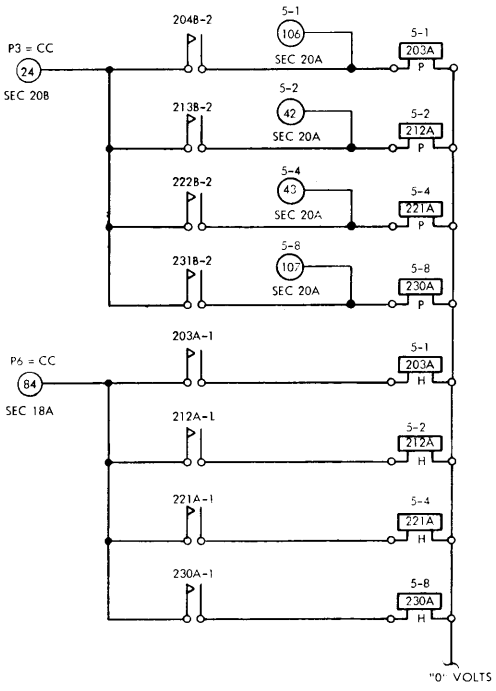
5393443

(FOR INSTRUCTIONAL USE ONLY)

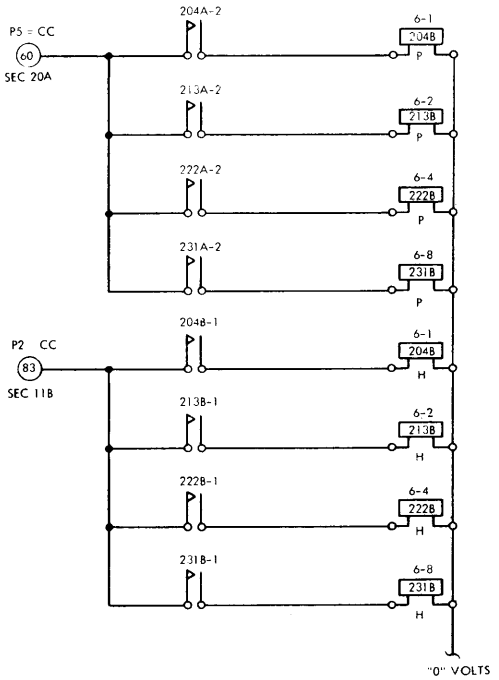
27
6TH REGISTER

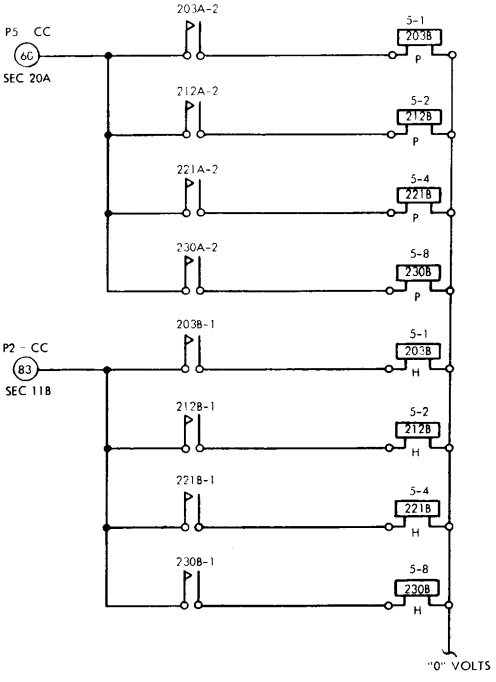


28
5TH REGISTER



A



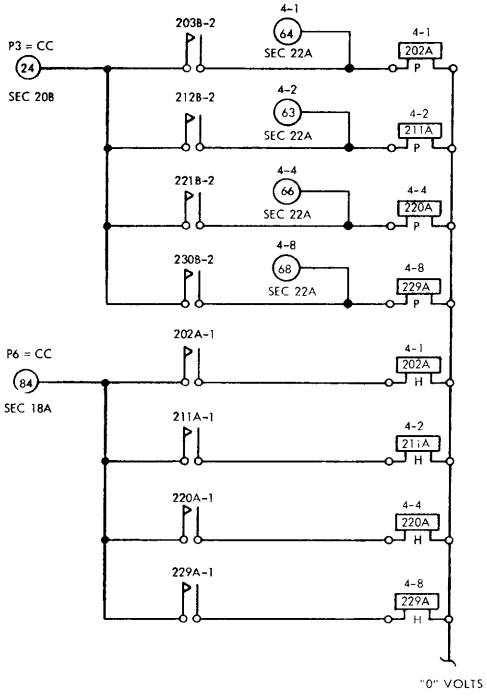


B

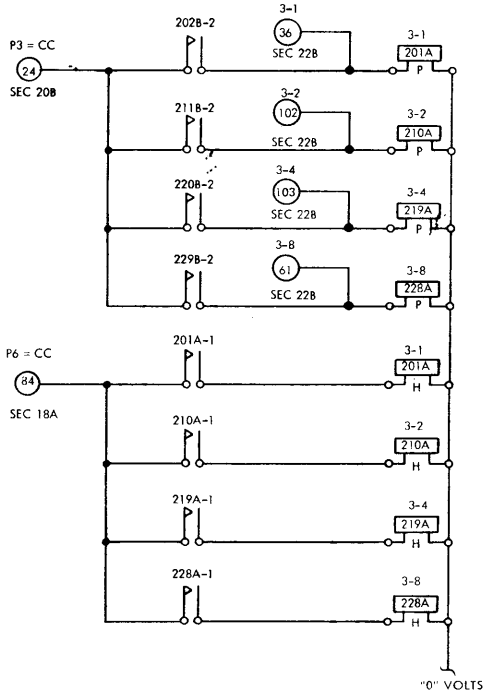
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5393444
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO.		
	01.29.12.1							895291		
DESIGN		MODEL								
DETAIL										
CHECK		DRAW							01.29.12.1	
APPRO		CHECK								

(FOR INSTRUCTIONAL USE ONLY)

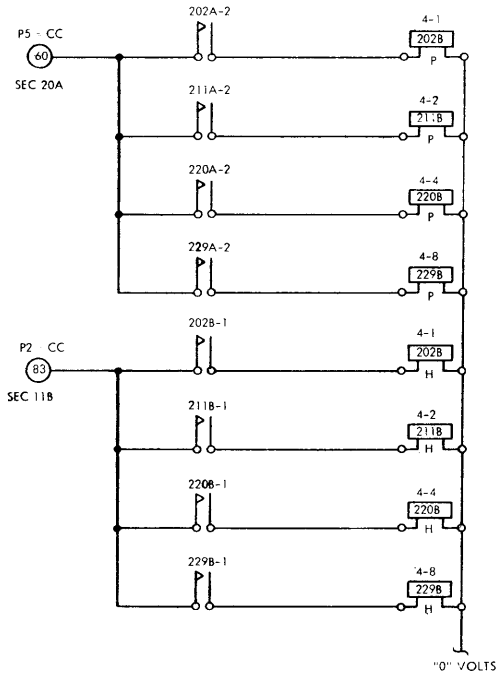
29 4TH REGISTER

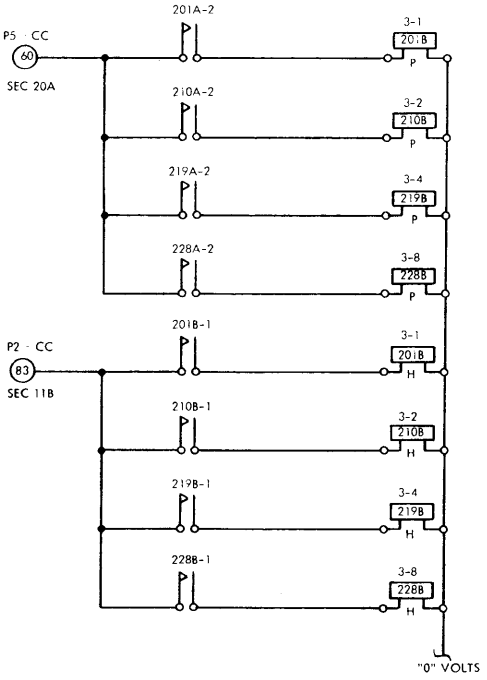


30 3RD REGISTER



A





B

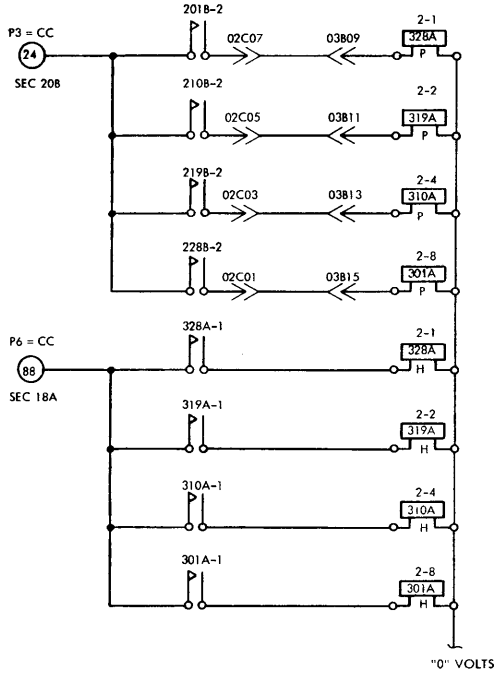
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.13.0								
DESIGN		MODEL							
DETAIL									01.29.13.1
CHECK		DRAW							
APPRO		CHECK							

5393446

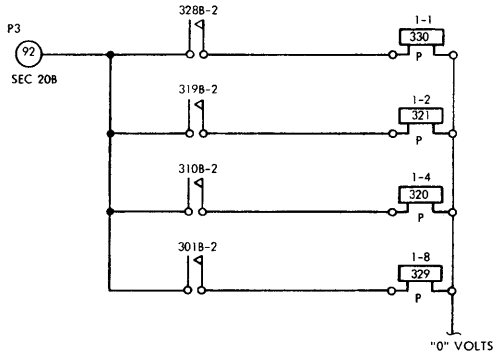
01.29.14.1

(FOR INSTRUCTIONAL USE ONLY)

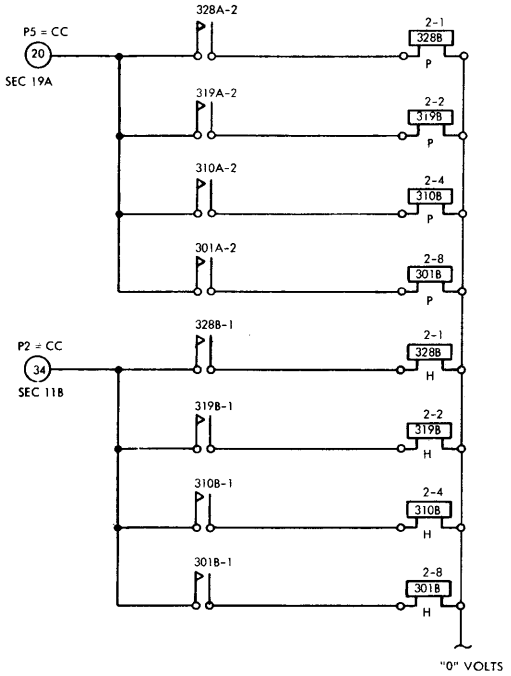
31 2ND REGISTER

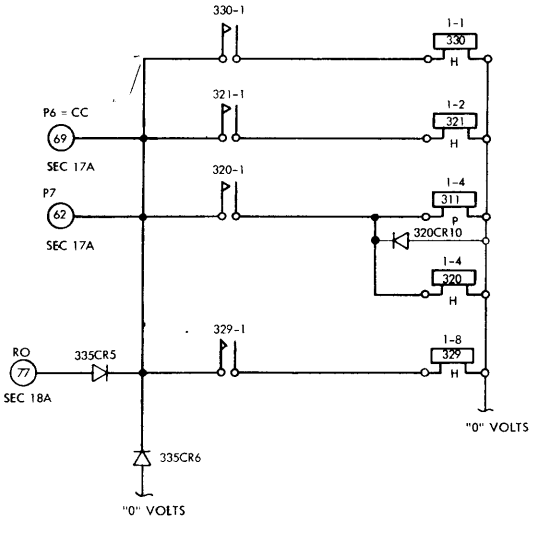


32 1ST REGISTER



A





B

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.14.1								
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							01.29.14.1
APPRO		CHECK							

5393446

(FOR INSTRUCTIONAL USE ONLY)

REED RELAYS

NAME	RELAY NO.	COIL P	COIL H	CONTACTS 1	2	3	4	5	6	PART NO.
ALPHA	104	12A		12A	1A	1A		9B		765726
PROG SEL	106	8A		9A	9A	11B	11B			765722
CLEAR 1	107	6B		6B	6A	5A	6A	5A	6B	765726
CLEAR 2	108	6A		5A	5A	6B			6B	765725
CARD LEVER	110	8B		9B		8A	5A			765722
PRINT	111	14A		14B	14B		14B			765722
CARD LEVER	112	8B		7B		9B	5A	1A	9A	765726
MULTI PUNCH	113	6A		5A	10A	9B	11B	10B	11A	765725
DUP 1	114	10A		7B	9B	9B	10A			765722
PROG SEL	115	8A		8A	9B	9B	9A	9A	8A	765726
DUP 1	116	10A		10A	11A	12B	10A			765700
SKIP	117	10A		7A						765825
DUP 2	120	10A		1B		10A	10A			765722
RELEASE	121	6B		10B	6B	5A		7B	9B	765726
DUP 2	122	10A		9B	11A	6A	10A			765722
SKIP	123	10B		9A	13B	10B	10A	11A	9B	765725
ESC INTLK	131	12A		11A	11A		9A	10A	10B	765725
1 BIT = 3RD REG	201A	30A	30A	30A	30B					765832
1 BIT = 3RD REG	201B	30B	30B	30B	31A					765832
1 BIT = 4TH REG	202A	29A	29A	29A	29B					765832
1 BIT = 4TH REG	202B	29B	29B	29B	30A					765832
1 BIT = 5TH REG	203A	28A	28A	28A	28B					765832
1 BIT = 5TH REG	203B	28B	28B	28B	29A					765832
1 BIT = 6TH REG	204A	27A	27A	27A	27B					765832
1 BIT = 6TH REG	204B	27B	27B	27B	28A					765832
1 BIT = 7TH REG	205A	26A	26A	26A	26B					765832
1 BIT = 7TH REG	205B	26B	26A	26B	27A					765832
1 BIT = 8TH REG	206A	25A		25A	25B					765832
1 BIT = 8TH REG	206B	25B	25B	25B	26A					765832
FIELD SIZE	208	18A		22A	22A	22A	22B	22B	22B	765820
FIELD SIZE	209	18A		22B	22B					765721
2 BIT = 3RD REG	210A	30A	30A	30A	30B					765832
2 BIT = 3RD REG	210B	30B	30B	30B	31A					765832
2 BIT = 4TH REG	211A	29A	29A	29A	29B					765832
2 BIT = 4TH REG	211B	29B	29B	29B	30A					765832
2 BIT = 5TH REG	212A	28A	28A	28A	28B					765832
2 BIT = 5TH REG	212B	28B	28B	28B	29A					765832
2 BIT = 6TH REG	213A	27A	27A	27A	27B					765832
2 BIT = 6TH REG	213B	27B	27B	27B	28A					765832
2 BIT = 7TH REG	214A	26A	26A	26A	26B					765832
2 BIT = 7TH REG	214B	26B	26B	26B	27A					765832
2 BIT = 8TH REG	215A	25A		25A	25B					765832
2 BIT = 8TH REG	215B	25B	25B	25B	26A					765832
FIELD SIZE	216	18A		22A	22A	22B	22B	22B	22B	765698
FIELD SIZE	217	18A		22B	22B	22B	22B	22A	22B	765725
FIELD SIZE	218	18B		22B	22B					765721
4 BIT = 3RD REG	219A	30A	30A	30A	30B					765832
4 BIT = 3RD REG	219B	30B	30B	30B	31A					765832

REED RELAYS

NAME	RELAY NO.	COIL P	COIL H	CONTACTS 1	2	3	4	5	6	PART NO.
4 BIT = 4TH REG	220A	29A	29A	29A	29B					765832
4 BIT = 4TH REG	220B	29B	29B	29B	30A					765832
4 BIT = 5TH REG	221A	28A	28A	28A	28B					765832
4 BIT = 5TH REG	221B	28B	28B	28B	29A					765832
4 BIT = 6TH REG	222A	27A	27A	27A	27B					765832
4 BIT = 6TH REG	222B	27B	27B	27B	28A					765832
4 BIT = 7TH REG	223A	26A	26A	26A	26B					765832
4 BIT = 7TH REG	223B	26B	26B	26B	27A					765832
4 BIT = 8TH REG	224A	25A		25A	25B					765832
4 BIT = 8TH REG	224B	25B	25B	25B	26A					765832
FIELD SIZE	226	18B		22A	22A	22A	22A	22A	22A	765820
FIELD SIZE	227	18B		22B	22A	22A	22A	22A	22B	765725
8 BIT = 3RD REG	228A	30A	30A	30A	30B					765832
8 BIT = 3RD REG	228B	30B	30B	30B	31A					765832
8 BIT = 4TH REG	229A	29A	29A	29A	29B					765832
8 BIT = 4TH REG	229B	29B	29B	29B	30A					765832
8 BIT = 5TH REG	230A	28A	28A	28A	28B					765832
8 BIT = 5TH REG	230B	28B	28B	28B	29A					765832
8 BIT = 6TH REG	231A	27A	27A	27A	27B					765832
8 BIT = 6TH REG	231B	27B	27B	27B	28A					765832
8 BIT = 7TH REG	232A	26A	26A	26A	26B					765832
8 BIT = 7TH REG	232B	26B	26B	26B	27A					765832
8 BIT = 8TH REG	233A	25A		25A	25B					765832
8 BIT = 8TH REG	233B	25B	25B	25B	26A					765832
FIELD SIZE	235	18B		22A	22A	22A	22A	22A	22A	765698
8 BIT = 2ND REG	301A	31A	31A	31A	31B					765832
8 BIT = 2ND REG	301B	31B	31B	31B	32A					765832
KEY ENTRY	304	18A		17B	21B	21B	21A	21B	21A	765698
PROG SEL	308	8A		17B	17B	17A	17A			765722
P CAM GATE	309	20B		20B	19A		20B			765722
4 BIT 2ND REG	310A	31A	31A	31A	31B					765832
4 BIT 2ND REG	310B	31B	31B	31B	32A					765832
4 BIT 1ST REG	311	32B		24B	24B	24A	24B			765722
FIELD 1	315	18A		1B	1B	1B	1B	1B	1A	765820
PUNCH OUT	317	20A		20A	19A	17B	19B			765722
2 BIT 2ND REG	319A	31A	31A	31A	31B					765832
2 BIT 2ND REG	319B	31B	31B	31B	32A					765832
4 BIT 1ST REG	320	32A	32B	32B	24A	24A	24A		24A	765729
2 BIT 1ST REG	321	32A	32B	32B	24A	24A	24A		24B	765729
FIELD 2	324	18A		1A	1A	1A	1A	19A	18A	765820
FIELD 3	325	18A		19A						765721
READ OUT	326	20A		19A	19A	19B	19B	18A	23A	765726
CR FIELD 2	327	20B		20B	19A	19B				765700
1 BIT 2ND REG	328A	31A	31A	31A	31B					765832
1 BIT 2ND REG	328B	31B	31B	31B	32A					765832
8 BIT 1ST REG	329	32A	32B	32B		23A	23A			765724
1 BIT 1ST REG	330	32A	32B	32B	24A	23A	24A		23A	765729
CR FIELD 1	336	20A		20B	19B	19A			20A	765725

WIRE CONTACT RELAYS

NAME	RELAY NO	COIL P	COIL H	CONTACTS 1	2	3	4	5	6	PART NO.
ESCAPE INTERLOCK	WCR-1	12A		10B			12A			328273

DIODES

RECT NO.	SEC	PART NO.
101CR1	2A	2111232
101CR2	13A	2111232
101CR3	2A	2111232
101CR4	13A	2111232
101CR5	2A	2111232
101CR6	13A	2111232
101CR7	2B	2111232
101CR8	13A	2111232
101CR9	2B	2111232
101CR10A	8A	2111232
101CR10B	13A	2111232
102CR1	2A	2111232
102CR2	13A	2111232
102CR3	2B	2111232
102CR4	13A	2111232
102CR5	2B	2111232
102CR6	13A	2111232
102CR7	2B	2111232
102CR8	13A	2111232
102CR9	2B	2111232
103CR3	2A	2111232
103CR7	2A	2111232
105CR1	7A	2111232
105CR5	8A	2111232
106CR1	6A	2111232
106CR10	8A	2111232
107CR10	5B	2106333
110CR2	14A	2106333
110CR10	8A	2111232
111CR1	14B	2106333
113CR10	5A	2106333
115CR2B	8A	2106333
116CR1	6B	2106333
116CR2	6B	2106333
117CR1	8B	2106333
117CR2	8B	2106333

DIODES

RECT NO.	SEC	PART NO.
117CR3	6A	2106333
117CR5	6A	2106333
119CR10	6A	2111232
120CR1	6B	2106333
120CR10	13B	2111232
122CR1	10A	2111232
122CR2	11A	2111232
122CR10	12A	2106333
123CR10B	10A	2111232
124CR3	7B	2111232
124CR4	9B	2111232
124CR8	9A	2111232
124CR9	10B	2111232
125CR2	12A	2106333
128CR10	13B	2111232
129CR4	10A	2106333
130CR10B	10A	2106333
132CR1	7A	2111232
132CR5	6B	2111232
132CR8	10B	2111232
133CR1	5B	2111232
134CR10	10B	2106333
301CR10	17A	2106333
303CR3	17B	2106333
303CR4	21B	2106333
303CR5	21B	2106333
303CR6	21B	2106333
303CR7	21B	2106333
303CR8	21B	2106333
305CR10	17B	2111232
307CR5	17A	2106333
307CR6	17A	2106333
307CR7	17A	2106333
307CR8	17A	2106333
307CR9	17A	2106333
307CR10	17A	2106333
308CR1	8A	2106333

DIODES

RECT NO.	SEC	PART NO.
308CR2	1B	2111232
309CR1	9A	2106333
308CR2	20B	2106333
314CR2	21A	2106333
314CR3	21A	2106333
314CR4	21A	2106333
314CR5	21A	2106333
314CR6	21A	2106333
314CR7	21A	2106333
314CR8	21A	2106333
314CR9	21A	2106333
316CR3	18B	2106333
316CR4	17A	2106333
316CR6		2106333
316CR10	20A	2106333
317CR10	20A	2106333
318CR1	11B	2106333
318CR2	11A	2106333
318CR3	19B	2106333
318CR4	17A	2106333
318CR7	20B	2106333
318CR5	17A	2106333
320CR10	20B	2106333
318CR9	19A	2111232
321CR10	18A	2106333
323CR2	21A	2106333
323CR3	21A	2106333
323CR4	21B	2106333
323CR5	21B	2106333
323CR6	21B	2106333
323CR7	21B	2106333
323CR8	21B	2106333
324CR10	19A	2106333
325CR1	19A	2106333
325CR2	19A	2106333
326CR10	12A	2106333
335CR1	20A	2106333
335CR2	20A	2106333
335CR3	20A	2106333
335CR5	32B	2106333
335CR6	32B	2106333

A

B

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	01.29.15.0							895291	
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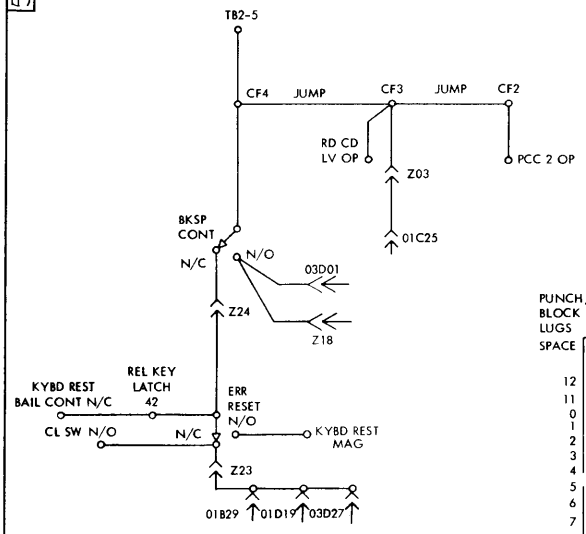
DETAIL									
CHECK		DRAW							01.29.15.0
APPRO		CHECK							

5393448

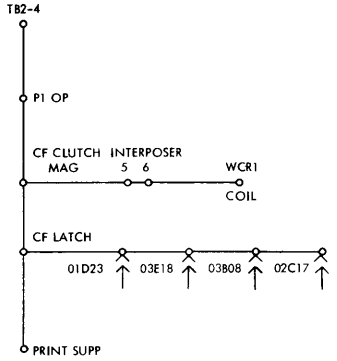
01.29.16.0

(FOR INSTRUCTIONAL USE ONLY)

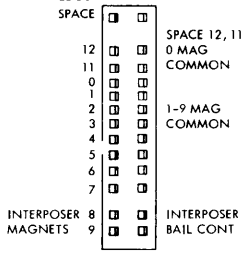
35 +48 VOLTS NET



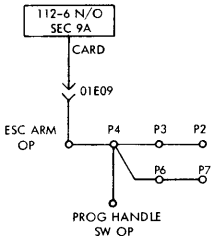
36 0 VOLTS NET



PUNCH UNIT TERMINAL BLOCK FACING WRINKLED LUGS



CD LV NET



A

CONNECTOR CHART

PIN	1A	1B	1C	1D	1E	2C	3B	3C	3D	3E	Z
1		14B	1A			31A		2B	18B		2A
2	6A	2A			11B		20B				1A
3	7A	11A			12A	31A		2B	1A	18A	35A
4	2A	2B	14B	8A			19A				1A
5		1B	5A	9B		31A			1A		1A
6	2A		1A	7A			11B		1B		1A
7	6A		6B			31A		17B	1A		1A
8	2A	2B	12B	6A	6A		36A			17A	1A
9	5A				11A		31A		1A	18B	1B
10	2B	2B	1A	9A	5A			2B		17A	1B
11	7B		1B	9B	9A		31A		1B	17A	1B
12	2B	2A	5A	9A	5B			2B			1A
13		2B	5A	9B	10A	11B	31A		1B		1B
14	2B	2B	1A	11B		18A		12A		17B	6A
15	9B	9B	6A	9A		20B	31A		1B		6A
16	2A	2B	1A	11B	5B			2A		17B	8B
17	1B	11B	9A	9A		36A			1B		8B
18	2A	2A			12B	19A	18A	2A		36A	8B
19			1A	8A		18A	18A		18A	8A	1B
20	2A	5B	10A		5B		21A	2A		1B	12B
21	7B		9B	9B	10A	18B			19A	19B	14B
22	2A	2A	7A	8A		18A	21B	2A		19B	9B
23	5A		8B	36A	5B		18A		1A	17A	35A
24	9B	2A	6A	10B		21B	21A	2A		9A	35A
25		1B	8A	6A			18B		19A	17A	
26	2B				8B	21B	21B				5B
27		9B	9A			21A			17B	10A	
28	2B	2A	5A	9A	11A			2B			
29	8A	5A	9B	12A		21A				11A	19A
30	2B		7A					2A	20B		18B

REED RELAY DATA

PART NO	COIL ROHMS	1	2	3	4	5	6
765698	1940	N/O	N/O	N/O	N/O	N/O	N/O
765700	3460	N/O	N/O	N/O	N/O		
765721	5735	N/O	N/O				
765722	3460	N/O	N/C	N/C	N/O		
765724	P 3045	N/O	N/C	N/C	N/O		
765724	H 3500	N/O	N/C	N/C	N/O		
765725	1940	N/O	N/C	N/C	N/C	N/C	N/O
765726	1940	N/O	N/O	N/C	N/C	N/O	N/O
765729	P 1815	N/O	N/O	N/C	N/C	N/O	N/O
765729	H 3085	N/O	N/O	N/C	N/C	N/O	N/O
765820	1940	N/C	N/C	N/C	N/C	N/C	N/C
765825	7385	N/O					
765832	P 4500	N/O	N/O				
765832	H 5700	N/O	N/O				

CARD FEED (CF) CAMS

NO.	LOC	PART NO	M	B
2	5B	309630	355° ± 2	180° ± 5
3	7B	309631	70° ± 2	150° ± 5
4	7A	309631	16° ± 2	96° ± 5

CAPACITORS

CAP	SEC	PART NO
128C4	1B	217077
134C1	10B	482145

PUNCH (P) CAMS

NO.	LOC	PART NO.	M	B
1	12A	309630	180° ± 1	0° ± 3
2	11A	309634	149° ± 3	790 ± 2
3	19B	227694	10° ± 1	60° ± 3
4	9A	309630	175° ± 3	355° ± 2
5	1B	309629	86° ± 3	166° ± 2
6	17A	326429	28° ± 2	158° ± 5
7	17A	308734	140° ± 5	10° ± 2

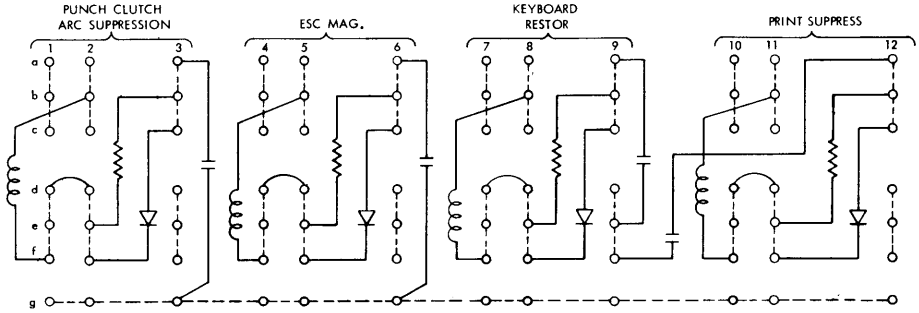
RESISTORS

RESISTORS	SEC	PART NO
128R1	1B	317428
115R10	8A	597682
134R4	10B	317014
128R4	2B	301149

B

ARC SUPP ASSEMBLIES

MAG	ARC SUPP PART NO
DIODE ASM	5400887
KYBD REST BAIL CONT	5372368
INDUCTOR ASM	5400916
CAPACITOR	5400889
CD FD CLUTCH MAG	2160917
RESISTOR ASM	5400888
ESC INTLK RLY	347820
CAPACITOR (SHORT LEAD) ASM	5400890



INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM							X PRINT TO ENG. SPEC. NO. 895291	
	01.29.16.0								
DESIGN		MODEL							
DETAIL									
CHECK		DRAW							
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